CAD Tools for 6.374

We will use three CAD tools for 6.374: Magic, HSPICE and Nanosim. Magic is used for drawing the layout of circuits. With the layout, we can perform extraction from layout to a HSPICE deck for simulation. The HSPICE deck contains information about the geometry of individual devices and parasitic capacitances of interconnects. It is similar to the HSPICE decks that you may use for the first problem set. This tutorial covers the basics of how to use Magic.

Magic Tutorial

Drawing a CMOS gate: 2-Input NAND

Task: Layout a 2-Input NAND gate with NMOS size 0.5/0.25 and PMOS size 0.75/0.25. Inputs should enter from the left in Poly and the output should exit the right in Poly. Power and Ground rails run vertically in Metal 1.

STEP 1: Plan your design.
In the space provided on the left, draw the circuit schematic for a 2-Input NAND gate. In the space on the right, sketch the layout for your design.
STEP 2: Starting to Layout - Drawing the NFETs
When you start Magic, a window should appear as shown in Figure 1. This is where you will draw your layout. The window in which you started ‘magic’ now becomes the console and logs all the commands and macros you type. Always point your mouse in the drawing window when you type a command or macro.

First, to facilitate your drawing, make the grid appear by typing ‘g’ (with the mouse in the drawing window.) You may not see the grid because the zoom is inappropriate. Type ‘v’ to zoom to the current selected object, which is a square. Type ‘Z’ to zoom out by a factor of 2 and ‘z’ to zoom in. The size of a small square is 1 λ.

Figure 1: Magic window.
Doing layout involves drawing rectangles and painting them to represent various layers. We will now draw an n-channel MOSFET (the uppermost one in the pair). At any point, to undo a the last step, type ‘u’.

**Step 1: Drawing the source, drain and channel region.**

Anchor one corner of a rectangle by clicking the left mouse button (in the Magic window). To select the other corner of the rectangle, click the right mouse button. (Make sure your mouse cursor looks like a cross-hair. If not, press space bar a few times until you see it.) Select a 17x4 rectangle. With the mouse in the window type (yes, include the ‘:’)

```
paint ndiff
```

You should see a green rectangle as shown in Figure 2

![Figure 2: Source, drain and channel region](image)

**Step2: Drawing the poly gate**

Using the same method, select a 2x8 rectangle overlapping the green rectangle. Type

```
paint poly
```

Add a second rectangle of poly three boxes away from the first.

You should see two red rectangles overlapping the green rectangle as shown in Figure 3. The overlapping regions are the channels of our two NFET devices.

![Figure 3: Poly gates over channel with source and drains on the side](image)

**Step 3. Drawing the M1 output contact**
Select a 4x4 rectangle on the right side of the green rectangle. Type
:paint ndc

This is a metal to n-diffusion contact. You do not need a contact on the source because it abuts directly with
the other NMOS device. Add a contact to the source of the second NMOS device (far left side).

Layer Names
The names of some various ‘layers’ are:
m1 - metal1
m2 - metal2
pdiff - p+ diffusion
pdc - p+ to metal 1 contact.
nwell - nwell for the p-channel MOSFET
nwc - nwell to metal1 contact
pwc - p substrate to metal1 contact
pc - poly to metal1 contact
m2c - metal1 to metal2 contact

Short-cuts for drawing
Instead of typing ':paint ...', once you have the basic layers on the drawing, you can copy and paste as fol-

Breaking and fixing design rules
When design rules are broken, magic gives a warning by covering the rectangle which has violated design
rules with an array of white dots.

In your drawing, select the tip of the poly and paint it gray. Type ‘y’ with the mouse in the dotted region to
see what design rule has been violated. In this case, the console reads:

Poly overhang of transistor < 2 (Mosis #3.3) [nfet,pfet space/
active,poly,pres,rp,pc/a poly,pres,rp,pc/a]

Practice breaking and fixing a few design rules. And now, BACK TO THE NAND GATE....

STEP 3 - Drawing the PFETs
Now draw the two PFETs above the NFETs. Give yourself LOTS of space for wiring and for meeting
design rules. To draw the PFETs, you will need to lay down an n-well, p-diffusion, poly, and contacts. Is
the location of the contacts the same as for the NFETs?

Figure 4 shows the layout with all four FETs in place.
STEP 4 - Wiring up the NAND gate

To connect metal to a via, just draw metal touching the via. For example, select a rectangle of at least 3x3 touching any contact. Type

```
paint m1
```

This paints a layer of metal 1.

Wire up the gates of the FETs in poly. You will have to jumper one of the gates in metal 1 to bring poly out to the left of the design. Now wire up the output node. Remember that you want to minimize capacitance at this node. Now wire up the power and ground. Are all of the connections in the circuit complete?

NO! You need to make contacts for the body terminals of your devices. Find the right type of contact in the layer list, and add the well contacts to your design.

STEP 5 - Labeling your circuit

Once your have drawn your circuit, you need to label the ports so that you can do an extraction of the layout into a circuit, including geometrical information and parasitics.
Click the middle of the VDD power strip with the left mouse button, followed by the right mouse button.
Type
\texttt{:label VDD!}

A label for VDD! appears. Do the same for the other nodes in the circuit.
You should get something like Figure 5 for your final layout. If you want to erase a label, select a rectangle containing the label and type
\texttt{:erase label}

Note: The ‘!’ in ‘VDD!’ represents that it is a global signal. It is the same when used in all instances. (Refer to the section on hierarchial designs about making instances of cells.)

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{nand_gate_labels.png}
\caption{NAND gate complete with labels}
\end{figure}
**STEP 6 - Saving, loading and extracting**

To save, type

```
:save tutorial
```

To load, type

```
:load tutorial
```

To extract the layout into a circuit for simulation in HSPICE and Irsim, type

```
:extract
```

This will create a file tutorial.ext which can be converted into a HSPICE deck and Nanosim deck using ext2spice and ext2sim respectively. We will discuss this later.

You can type

```
:quit
```

to exit Magic.

**STEP 7 - Creating and Verifying your netlist**

Convert the layout to a spice netlist. View the netlist to see if it looks correct.

Are there any problems?

You will find that CAD tools **never** do everything you would like. For example, the netlist sizes devices in terms of a scaled unit, but it uses the wrong scale unit! Also, the names of the FETs are nfet and pnet, not nch and pch. VLSI designers become masters at writing scripts to tie together CAD tools and to make things work.

**More short cuts for drawing**

**Selecting and Moving**

You may want to move certain blocks. To select a rectangle, point the mouse over the rectangle and type ‘s’. To select a whole region, select a rectangle, and type ‘a’.

Once a rectangle or block is selected, you can move them by typing ‘q’ for left, ‘w’ for down, ‘e’ for up and ‘r’ for right.

**Hierarchy in designs**

In the layout of complex circuits, hierarchy is very useful to maintaining modularity. For example, an 8-bit adder can be made from an array of 1 bit adders. However, to be able to do this, it is necessary to layout cells so that they can be made into modules by putting them next to each other.

Here is an example of how to create an array of cells:

```
:getcell name
```

finds the file name.mag on disk, reads the cell it contains, and creates an instance of that cell.

To turn the instance into an array, invoke the command:
:array xsize ysize
where xsize and ysize indicates how many elements the array should have in the x- and y-direction respectively.

To see the layout in individual cells, use the command :expand all.

Here is how to generate an array of your nand gate:
Step 1. Layout the nand gate and save it with a name like ‘tutorial’.
Step 2. Use the command :getcell tutorial to create an instance of the nand gate.
Step 3. Use the command :array 3 1 to make an array 3 by 1 of the gate.
Step 4. Use the :expand to display the layout of each cell.

You probably would need to modify the original cell so that the inputs and outputs meet up correctly.
I. Basic Usage of HSPICE and Awaves

Step 1. Create an HSPICE file

All HSPICE files should have an .sp extension.

Type in athena prompt:
% emacs inv.sp &

Simple HSPICE file:

*CMOS Inverter - DC Sweep

* Netlist

* Define Voltage Sources
  vdd 1 0 2.5
  vin in 0 pvdd

* Define Transistors
  m1 out in 1 1 pch l=0.25u w=1.125u as=0.7p ad=0.7p ps=2.375u pd=2.375u
  m2 out in 0 0 nch l=0.25u w=0.375u as=0.7p ad=0.7p ps=2.375u pd=2.375u

* Define Output Capacitance
  Cout out 0 30f

* Define Parameters
  .param pvdd=2.5V

* Models
  .lib 'logic025.l' TT

* Analysis

* post option necessary for awaves
  .options nomod post
* DC sweep from 0 to 2.5V at 0.01V increments
  .dc vin 0 pvdd 0.01

.end

-----------------------------

Simple HSPICE file2:
-----------------------------
*CMOS Inverter - Transient Analysis

* Netlist

* Define Voltage Sources
vdd 1 0 2.5
vin in 0 pulse(0v 2.5v 1n 0.1n 0.1n 4n 8n)

* Define Transistors
m1 out in 1 1 pch l=0.25u w=1.125u as=0.7p ad=0.7p ps=2.375u pd=2.375u
m2 out in 0 0 nch l=0.25u w=0.375u as=0.7p ad=0.7p ps=2.375u pd=2.375u

* Define Output Capacitance
Cout out 0 30f

* Models
.lib 'logic025.l' TT

* Analysis

* post option necessary for awaves
.options nomod post

* Transient Analysis for 10ns
.tran 0.01n 10n

.end

-----------------------------

There are three main sections in the file:

a. the netlist: Netlist is a designation for a computer readable representation of the circuit schematic.
b. the models: A model in spice is a description of the parameters of the equations used by spice to analyze the circuit.
c. the analysis to be performed: here we are requesting a DC sweep from 0 to 2.5 with 0.01V increments and a transient analysis for 10 ns with step 0.01n.
d. the end of the file. This isn’t really a main section, but hspice won’t work without it, and many people forget about it. Always put a .end statement at the end of your file.

Step 2.

If you haven’t done so, add spice (this command also adds awaves):
% add hspice

Run spice in the background, and direct the output to a file for later reference:
% hspice inv.sp > inv.out &

When the simulation is complete, you should have some *.sw* (DC “sweep” data) and/or *.tr* (transient analysis data) files:
% ls
inv.sp      inv.out      inv.sw0      inv.tr0

**Step 3.**

Now, we use awaves to display the data generated by hspice stored in the .sw and .tr files:
% awaves inv &

To view waveforms, select the node number (or node name) that you want to see with the mouse button and drag and drop them in the highlighted panel. Double-clicking on the node numbers also brings up the waveforms. Panels are highlighted when they have a red border. The graph window will display the waveforms which can be measured using a variety of features.

**NOTE:** awaves doesn’t run on Linux.
Sample Inverter Layout
Basic Usage of Magic

The Basics

1. Changing tools

There are 4 types of tools you can select in magic by pressing the space bar. The one that is used most often is the box tool, which the mouse cursor looks like a cross hair. You should be using box tool when you are designing basic transistor cells.

: Box Tool
2. Commands

Commands can be invoked in Magic in three ways: 1) by pressing buttons on the mouse; 2) by typing single key-strokes on the keyboard (called macros); 3) typing longer commands on the keyboard (called long commands).

When you're giving commands, make sure that the mouse cursor is on the cell window, not on the command window. Long commands are invoked by typing a colon (:). After you type the colon or semi-colon, the “>” prompt on the command window will be replaced by “:”. (When you're giving macro or mouse commands, the cursor on the command window should be “>”)

Most of the commands that we will be using are the default macros. In general, commands are sent to MAGIC using the format “: [keyword] [arguments]”. To see a list of commands or to get help on a particular, use the “:help [keyword]” command.

3. Viewing

The first thing you should do is show the grid. Typing “g” will turn the grid on/off. (or “:grid 1” (1 lambda per division) or “:grid 2” (2 lambda per division)). Here are some ways to view the cell.

<table>
<thead>
<tr>
<th>Macro Command</th>
<th>Long Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>v</td>
<td>:view</td>
<td>View the entire cell.</td>
</tr>
<tr>
<td>z</td>
<td>:zoom 2</td>
<td>Zooms in to the area specified by rectangle</td>
</tr>
<tr>
<td>Z</td>
<td></td>
<td>Zooms out by a scale factor of 2</td>
</tr>
<tr>
<td>,</td>
<td></td>
<td>Centers screen about mouse cursor, keeping zoom factor constant</td>
</tr>
</tbody>
</table>

Painting Layers / Design Rules

You will need to draw rectangles a lot. To draw them, use the left mouse button to set one of the corners, and the right mouse button to set the other. If you already have a rectangle drawn, clicking the left mouse button moves the rectangle and with its origin (the lower left corner) at the cursor location. Clicking the right mouse button will change the position of the other corner of the rectangle, while keeping the origin at the same point. This is useful for resizing box sizes. Practice this a little. The middle mouse button copies all the layers under the mouse cursor location to the currently drawn box. (more on this later.)

Now you're ready to draw the transistors. In general, it's best to save drawing the wells (pwell and nwell) for last. Specify a box about 5 lambda tall and 1 lambda wide. Now, type “:paint poly”. Note that the box is now red, which is poly. Note also that white dots have appeared next to it. This means that you have violated a design rule. To find out exactly what design rule you have violated, draw a box containing some white dots and press “y”. Some information regarding the drc (design rule check) violation(s) will be displayed in the text window.

Once you have drawn a piece of poly, you no longer need to type “:paint poly”. All you need to do is to draw another box of poly (or any other layer) to specify a new box, then move your mouse pointer to the layer(s) to be copied into the box and press the middle mouse button. Remember, however that all the layers will be copied; a common mistake is to copy multiple layers by accident.

^D is the converse of the middle mouse button; pressing ^D will delete all the layers under the mouse cursor from the currently specified box.

Here are some of the more common paint layers:

Single layers

<table>
<thead>
<tr>
<th>Single layer</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>p or poly or polysilicon or red</td>
<td>Polysilicon</td>
</tr>
<tr>
<td>blue or m1 or metal1</td>
<td>Metal 1</td>
</tr>
<tr>
<td>m2 or metal2 or purple</td>
<td>Metal 2</td>
</tr>
<tr>
<td>cyan or m3 or metal3</td>
<td>Metal 3</td>
</tr>
</tbody>
</table>
green or ndiff or ndiffusion  n-type diffusion (for use w/ NMOS)
brown or pdiff or pdiffusion  p-type diffusion (for use w/ PMOS)
pw or pwell p-well (for use w/ NMOS)
nw or nwell n-well (for use w/ PMOS)

Complex layers
nfet or ntransistor  Poly over ndiffusion (NMOS)
pfet or ptransistor  Poly over pdiffusion (PMOS)

Contacts
pc or pcontact or polycontact or polycut  Poly to Metal1
m2c or m2contact or m2cut or v or via  Metal1 to Metal2
m3c or m3contact or m3cut or v2 or via2  Metal2 to Metal3
ndc or ndcontact or ndiffcut  n-diffusion to Metal1
pdc or pdcontact or pdiffcut  p-diffusion to Metal2
pwc or pwcontact  p-well to Metal1 (for well contacts, usually)
nwc or pwcontact  n-well to Metal1 (for well contacts, usually)

Editing / Moving Rectangles

To edit or move objects, you must specify them. This is how:

s  select the largest box containing all the layers under the mouse cursor.
S  keep the current selection and add another box containing all the layers under the current cursor position.
a  select everything under the specified box.

d  delete selected object
c  copy selected object (distance from origin of box to cursor position specifies where copy is placed)
m  move selected object (distance from origin of box to cursor position specifies where object is placed)

e  q  r  direction to move a selected object by 1 lambda
w
E
Q  R  direction to stretch a selected object by 1 lambda
W

Magic has a large undo/redo buffer. Paint, move and experiment with these options:

u  undo
U  redo

Finally, don’t forget to save your work:

:save mylayout

The filename will be called “mylayout.mag”.

There are still many topics not covered; only the very basics were covered. Reading the magic tutorials is highly recommended.

Step 3.
Layout an inverter following the attached layout. Once your layout is done, we need to extract the circuit for simulation. If you used the technology file option when you started magic, the extraction style should default to the standard for 6.374. Simply type the following:

```
:extract
```

This will create a “filename.ext” file that can be used by ext2spice and ext2sim.

**Step 4.**

To simulate a circuit in HSPICE, run ext2spice on the .ext file:

```
The
% ls
inverter.ext  inverter.mag

% ext2spice inverter

% ls
inverter.ext  inverter.mag  inverter.spice
```

The .spice file will only have transistor information (parasitic R and C are included); voltage sources, .model statements, .sweep and .tran statements must all be added.

The macros are listed below for your convenience:

- Macro `'^D' contains ``erase $'' (erase layer(s) under cursor from sel. region)
- Macro `'^L' contains ``redraw''
- Macro `'^N' contains ``iroute route -dSelection''
- Macro `'^R' contains ``iroute route -dBox''
- Macro `'^X' contains ``expand toggle''
- Macro `'' contains ``tool''
- Macro `',,' contains ``center''
- Macro `'.,' contains ``macro'' (repeat last command)
- Macro `'?'' contains ``help''
- Macro `'A'' contains ``select more area''
- Macro `'B'' contains ``findbox''
- Macro `'C'' contains ``select clear''
- Macro `'E'' contains ``stretch up 1''
- Macro `'G'' contains ``grid 2''
- Macro `'O'' contains ``closewindow''
- Macro `'Q'' contains ``stretch left 1''
- Macro `'R'' contains ``stretch right 1''
- Macro `'S'' contains ``select more''
- Macro `'T'' contains ``stretch''
- Macro `'U'' contains ``redo''
- Macro `'W'' contains ``stretch down 1''
- Macro `'X'' contains ``unexpand''
- Macro `'Z'' contains ``zoom 2''
- Macro `'a'' contains ``select area''
- Macro `'b'' contains ``box''
- Macro `'c'' contains ``copy''
- Macro `'d'' contains ``delete''
Macro 'e' contains "move up 1"
Macro 'f' contains "select cell"
Macro 'g' contains "grid"
Macro 'o' contains "openwindow"
Macro 'q' contains "move left 1"
Macro 'r' contains "move right 1"
Macro 's' contains "select"
Macro 't' contains "move"
Macro 'u' contains "undo"
Macro 'v' contains "view"
Macro 'w' contains "move down 1"
Macro 'x' contains "expand"
Macro 'y' contains "drc why"
Macro 'z' contains "findbox zoom"

EXAMPLE

INVERTER

athena % magic

Magic 6.4.4 - Compiled on Wed Jun 21 00:22:15 EDT 1995.
Using technology "scmos", version 8.2.6.
MOSIS Scalable CMOS Technology for Standard Rules
Unable to allocate 7 planes in default colormap; making a new one.
Black = 0       White= 1
Using new basepixel = 128
Only 126 contiguous colors were available.

Magic news (07 Jun 1995):

Rev. 8.2.6 of the MOSIS SCMOS technology file is now installed.
<jgealow@mtl>

If you need help using Magic, send mail to cad-problems@mtl.

> :paint pdiff
  :paint ndiff
  :paint poly
  :paint pdc
  :paint ndc
  :paint pc
  :paint ml
  :label IN left pc
  :label OUT right ml
  :label Vdd! center ml
  :label GND! center ml
Selected cell is inv (Topmost cell in the window)
:save inverter
:extract style SCNE12(ORB)
Extraction style is now "SCNE12(ORB)"
:extract all
Extracting inverter into inverter.ext:
:quit

athena %
The following table shows parameter values for the minimum-sized NMOS and a similarly sized PMOS device in our generic 0.25 μm CMOS process. We will use the following parameters in this course.

Parameters for manual model of generic 0.25 μm CMOS process (minimum sized device).

<table>
<thead>
<tr>
<th></th>
<th>$V_{T0}$ (V)</th>
<th>$\gamma (V^{0.5})$</th>
<th>$V_{DSAT}$ (V)</th>
<th>$k'$ (A/V²)</th>
<th>$\lambda (V^{-1})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>$115 \times 10^{-6}$</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-30 \times 10^{-6}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

With the above conventions, the $I_D$ equation presented in the previous viewgraph can be used for PMOS devices with $I_{DP}$ defined as the current going into the drain terminal. $V_{min}$ should be changed to $V_{max} = \max (V_{GT}, V_{DS}, V_{DSAT})$.
Unless otherwise specified, use the 0.25 micron libraries for all HSPICE simulations.

**Problem 1: Device Parameters**

The data from five measurements made on a short channel NMOS device appears in Table 1. Given that $V_{DSAT} = 0.6 \, V$ and $k' = 100 \, \mu A/V^2$, calculate $V_{TH}$, $\gamma$, $2/\phi_F$, and $W/L$.

<table>
<thead>
<tr>
<th>Meas. Number</th>
<th>$V_{GS}$</th>
<th>$V_{DS}$</th>
<th>$V_{BS}$</th>
<th>$I_D (\mu A)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.5</td>
<td>1.8</td>
<td>0</td>
<td>1812</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>1.8</td>
<td>0</td>
<td>1297</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>2.5</td>
<td>0</td>
<td>1361</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>1.8</td>
<td>-1</td>
<td>1146</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>1.8</td>
<td>-2</td>
<td>1039</td>
</tr>
</tbody>
</table>

**Problem 2: Backgate Effect**

The circuit in Fig. 1 is known as the *source follower* configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current $I_0$. Assume $x_d=0$, $\gamma=0.4$, $2/\phi_F=0.6\, V$, $V_{TH}=0.43\, V$, $k_n'=115 \, \mu A/V^2$ and $\lambda=0$.

![Figure 1: NMOS source follower configuration](image-url)
a) Suppose we want the nominal level shift between $V_i$ and $V_o$ to be 0.6V in the circuit in Figure 1(a). Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate $V_i$ to $V_o$ in terms of $I_o$).

b) Now assume that an ideal current source replaces M2 (Figure 1(b)). The NMOS transistor M1 experiences a shift in $V_T$ due to the backgate effect. Find $V_T$ as a function of $V_o$ for $V_o$ ranging from 0 to 2.5V with 0.5V intervals. Plot $V_T$ vs. $V_o$.

c) Plot $V_o$ vs. $V_i$ as $V_o$ varies from 0 to 2.5V with 0.5V intervals. Plot two curves: one neglecting the backgate effect and one accounting for it. How does the backgate effect influence the operation of the level converter?

At $V_o$(with backgate effect) = 2.5V, find $V_o$(ideal) and thus determine the maximum error introduced by the backgate effect.

**Problem 3: Velocity Saturation**

This problem explores the behavior of short-channel devices. For the HSPICE simulations of this problem you will use the 0.18um model parameters. Use the HSPICE model parameters which can be found in “log018_1.1”

a) Using HSPICE plot $I_D$ versus $V_{DS}$, for the transistor of the following figure, with $V_{GS}$ (0.6V, 0.8V, 1V, 1.2V, 1.4V, 1.6V, 1.8V) as a parameter. Comment on the dependence of $I_D$ with respect to $V_{GS}$.

![Short channel Transistor.](image)

b) Calculate the effective resistance for a high to low transition, using the method described in slide 44 (Handout 2).

c) Consider two CMOS inverters with $(W_1/L_1)_n$=(2.88u/1.44u), $(W_1/L_1)_p$=(5.76u/1.44u) and $(W_2/L_2)_n$=(0.36u/0.18u), $(W_2/L_2)_p$=(0.72u/0.18u). Assume $V_{DD}$ = 1.8 V and the output of the inverter is loaded by $C_L$=100fF capacitance. Calculate the propagation delay $t_p$ and check the answers with HSPICE.

d) Repeat part c) sweeping the supply voltage $V_{DD}$ from 0.4V to 1.8V (sweep step 0.2V). Plot the propagation delay $t_p$ versus the supply voltage $V_{DD}$ in the same graph. Comment on the results.

**Problem 4: Voltage transfer characteristics, Noise Margins**

The next figure shows an all NMOS inverter.
a) Calculate $V_{OH}$, $V_{OL}$, and $V_M$ for the new inverter.

$$V_{DD} = 2.5V$$

$$M_2 \quad W/L=0.375/0.25$$

$$V_{OUT}$$

$$V_{IN} \quad M_1 \quad W/L=0.75/0.25$$

**Figure 3: An Alternate Inverter Implementation**

b) Use HSPICE to obtain the VTC.

c) Calculate $V_{IH}$, $V_{IL}$, and the noise margins and comment on the results. How can you increase the noise margins and reduce the undefined region?

d) Comment on the differences in the VTCs, robustness, and regeneration between this inverter and a standard CMOS inverter.

**Problem 5: Inverter Gain and Regions of Operation**

The Figure 4 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at $V_M$. The intersection of this line with the $V_{OH}$ and the $V_{OL}$ lines defines $V_{IH}$ and $V_{IL}$.

**Figure 4: A Different Approach to Derive $V_{IL}$ and $V_{IH}$**
a) The noise margins of a CMOS inverter are highly dependent on the sizing ratio, \( r = \frac{k_p}{k_n} \), of the NMOS and PMOS transistors. Use HSPICE with \( V_{Tn} = |V_{Tp}| \) to determine the value of \( r \) that results in equal noise margins? Give a qualitative explanation.

b) Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for \( NM_H \) and \( NM_L \) in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at \( V_M \). For what range of \( r \) is this assumption valid? What is the resulting range of \( V_M \)?

c) Use the method from section 5.3.2 to derive an expression for the inverter gain at \( V_M \) for the case when the sizing ratio is chosen to place \( V_M \) just below limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS?

Problem 6: Static CMOS Inverter

For this problem use scalable CMOS design rules and assume:

\[
V_{DD} = 2.5V, \quad W_P/L = 1.25/0.25, \quad W_N/L = 0.375/0.25, \quad L = L_{eff} = 0.25\mu m \quad (i.e. \quad x_{id} = 0\mu m), \quad C_L = C_{inv-gate}, \quad k_n' = 115\mu A/V^2, \quad k_p' = -30\mu A/V^2, \quad V_{tn0} = |V_{tp0}| = 0.4V, \quad \lambda = 0V^{-1}, \quad \gamma = 0.4, \quad 2|\phi_f| = 0.6V, \text{ and } t_{ox} = 58A. \text{ Use the Hspice model parameters for parasitic capacitance given below (i.e. } C_{gd0}, C_{j}, C_{jsw}), \text{ and assume that } V_{SB} = 0V \text{ for all problems except part (e).}
\]

Figure 5: CMOS inverter with capacitive load.

## Parasitic Capacitance Parameters (F/m)##

**NMOS**

\[
C_{gd0} = 3.11 \times 10^{-10}, \quad C_{gs0} = 3.11 \times 10^{-10}, \quad C_J = 2.02 \times 10^{-3}, \quad C_{JSW} = 2.75 \times 10^{-10}
\]

**PMOS**

\[
C_{gd0} = 2.68 \times 10^{-10}, \quad C_{gs0} = 2.68 \times 10^{-10}, \quad C_J = 1.93 \times 10^{-3}, \quad C_{JSW} = 2.23 \times 10^{-10}
\]

a) What is the \( V_m \) for this inverter?

b) What is the effective load capacitance \( C_{L_{eff}} \) of this inverter? (include parasitic capacitance, refer to notes for \( K_{eq} \) and \( m \).) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, \( \lambda = 0.125 \mu m \), and the source/drain extensions are 5\( \lambda \) for the PMOS; for the NMOS the source/drain contact regions are 5 \( \lambda \).
c) Calculate $t_{PHL}$, $t_{PLH}$ assuming the result of (b) is ‘$C_{Eff} = 6.5\text{fF}$’. (Assume ideal step input, i.e. $t_{rise}=t_{fall}=0$. Do this part by computing the average current used to charge/discharge $C_{Eff}$.)

d) Find $(W_p/W_n)$ such that $t_{PHL} = t_{PLH}$.

e) Suppose we increase the width of the transistors to reduce the $t_{PHL}$, $t_{PLH}$. Do we get a proportional decrease in the delay times? Justify your answer.

f) Suppose $V_{SB} = 1V$, what is the value of $V_{tn}$, $V_{tp}$, $V_m$? How does this qualitatively affect $C_{Eff}$?

g) Use Magic to create a layout for this inverter. Extract the schematic, including parasitic capacitance, from the layout and use HSPICE to simulate the circuit and measure $t_p$ and the average power for the following input $V_{in}$: pulse(0 $V_{DD}$ 5n 0.1n 0.1n 9n 0.1n 20n), as $V_{DD}$ varies from 1V - 2.5V with 0.25V interval. [$t_p = (t_{PHL} + t_{PLH}) / 2$]. Using this data, plot ‘$t_p$ vs. $V_{DD}$’, and ‘Power vs. $V_{DD}$’.

The extracted layout will include parasitics so you need not manually include AS, AD, PS, PD in your spice deck, but remember to manually add $C_L = 6.5\text{fF}$. Set $V_{SB} = 0V$ for this problem. Use the HSPICE model parameters which can be found in “logic025.l”.

h) Using HSPICE, simulate the circuit for a set of ‘pulse’ inputs with rise and fall times of $t_{rise,fall}=1\text{ns}$, 2ns, 5ns, 10ns, 20ns. For each input, measure (1) the rise and fall times $t_{out,rise}$ and $t_{out,fall}$ of the inverter output, (2) the total energy lost $E_{total}$ and (3) the energy lost due to short circuit current $E_{short}$. For measuring short circuit power, use the technique discussed in class (slide 96, Handout 2). Use the HSPICE model parameters which can be found in “logic025.l”.

Using this data, prepare a plot of (1) $(t_{out,rise}+t_{out,fall})$ vs. $t_{in,rise,fall}$, (2) $E_{total}$ vs. $t_{in,rise,fall}$, (3) $E_{short}$ vs. $t_{in,rise,fall}$ and (4) $E_{short}/E_{total}$ vs. $t_{in,rise,fall}$.

Provide simple explanations for:
(i) Why the slope for (1) is less than 1?
(ii) Why $E_{short}$ increases with $t_{in,rise,fall}$?
(iii) Why $E_{total}$ increases with $t_{in,rise,fall}$?
Problem 1: Device Parameters

The data from five measurements made on a short channel NMOS device appears in Table 1. Given that $V_{DSAT} = 0.6 \, V$ and $k' = 100 \, \mu A/V^2$, calculate $V_{T0}$, $\gamma$, $2/\phi_F$, and $W/L$.

Table 1: Measured Data for Short Channel NMOS

<table>
<thead>
<tr>
<th>Meas. Number</th>
<th>VGS (V)</th>
<th>VDS (V)</th>
<th>VBS (V)</th>
<th>ID (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.5</td>
<td>1.8</td>
<td>0</td>
<td>1812</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>1.8</td>
<td>0</td>
<td>1297</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>2.5</td>
<td>0</td>
<td>1361</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>1.8</td>
<td>-1</td>
<td>1146</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>1.8</td>
<td>-2</td>
<td>1039</td>
</tr>
</tbody>
</table>

Solution

Using the data from the table, set up equations containing the unknowns of interest. We will use the unified MOSFET model for our analysis: $k_n W/L (V_{GT} V_{DSAT} V_{T0}^2/2)(1 + \lambda V_{DS}) = I_o$.

Let us first make an assumption about the region of operation. The minimum $V_{DS}$ is greater than $V_{DSAT}$. Unless $V_{T0}$ is abnormally high, the device is in the velocity saturation region for all the data points. We can check this assumption at the end of the problem. Using this assumption, the first three data points give us the following equations:

$$100 \cdot \frac{W}{L} \cdot \left(2.5 - V_{T0}\right) \cdot 0.6 - \frac{0.6^2}{2} \cdot (1 + \lambda \cdot 1.8) = 1812 \mu A$$

$$100 \cdot \frac{W}{L} \cdot \left(2 - V_{T0}\right) \cdot 0.6 - \frac{0.6^2}{2} \cdot (1 + \lambda \cdot 1.8) = 1297 \mu A$$

$$100 \cdot \frac{W}{L} \cdot \left(2 - V_{T0}\right) \cdot 0.6 - \frac{0.6^2}{2} \cdot (1 + \lambda \cdot 2.5) = 1361 \mu A$$

These are three equations with three unknowns - piece of cake! Divide the first two equations to get:

$$\frac{(2.5 - V_{T0}) \cdot 0.6 - \frac{0.6^2}{2}}{(2 - V_{T0}) \cdot 0.6 - \frac{0.6^2}{2}} = \frac{1812}{1297}.$$  Simplifying gives: $1.5 - 0.6V_{T0} - 0.18 = 1.397 \cdot (1.2 - 0.6V_{T0} - 0.18)$

and $0.2382V_{T0} = 0.1049$ and $V_{T0} = 0.44 \, V$. 

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Dividing the second and third equations gives:
\[
\frac{1 + \lambda \cdot 1.8}{1 + \lambda \cdot 2.5} = \frac{1297}{1361}
\]
Solving for \(\lambda\) gives \(\lambda = 0.08\).

Plugging these two parameters into the first equation gives: \(\frac{W}{L} = 15\).

Writing two equations from the last two data points permits us to solve for the remaining two unknowns:
\[
1716 \cdot (2 - V_{T1}) \cdot 0.6 - 0.18 = 1146 \quad \text{so} \quad V_{T1} = 0.5869.
\]
\[
1716 \cdot (2 - V_{T2}) \cdot 0.6 - 0.18 = 1039 \quad \text{so} \quad V_{T2} = 0.6909.
\]

Now we use the equation for threshold voltage to relate the remaining unknowns:
\[
0.44 + \gamma \cdot (\sqrt{2\phi_F} + 1 - \sqrt{2\phi_F}) = 0.5869
\]
\[
0.44 + \gamma \cdot (\sqrt{2\phi_F} + 2 - \sqrt{2\phi_F}) = 0.6909
\]

Subtracting 0.44 from both sides and dividing the equations gives:
\[
\frac{\sqrt{2\phi_F} + 2 - \sqrt{2\phi_F}}{\sqrt{2\phi_F} + 1 - \sqrt{2\phi_F}} = 1.7.
\]
Simplifying gives: \(1.7 \cdot \sqrt{2\phi_F} + 1 = \sqrt{2\phi_F} + 2 + 0.7 \cdot \sqrt{2\phi_F} \).

Squaring both sides gives: \(2.89 \cdot (2\phi_F + 1) = 2\phi_F^2 + 2 + 1.4 \cdot \sqrt{2\phi_F} + 0.49 \cdot 2\phi_F + 1.4 \cdot \sqrt{2\phi_F} \).

Collecting terms gives: \(1.4 \cdot 2\phi_F + 0.89 = 1.4 \cdot \sqrt{2\phi_F} + 2 \cdot 2\phi_F \). Squaring both sides and solving gives: \(2\phi_F = 0.556\).

We can plug this value back into either threshold voltage equation to get \(\gamma = 0.293\).

**Problem 2: Backgate Effect**

The circuit in Fig. 1 is known as the *source follower* configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current \(I_0\). Assume \(x_d=0, \gamma=0.4, 2\phi_F=0.6\,\text{V}, V_{T0}=0.43\,\text{V}, k_n=115\,\mu\text{A/V}^2\) and \(\lambda=0\).

![Figure 1: NMOS source follower configuration](image.png)

a) Suppose we want the nominal level shift between \(V_i\) and \(V_o\) to be 0.6\,\text{V} in the circuit in Figure 1(a).
Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate $V_i$ to $V_o$ in terms of $I_o$).

**Solution**

The level shift of 0.6 tells us that $V_{GS1} = 0.6$ so $V_{GT1} = 0.17$. This means that M1 must be in the saturation region (not velocity saturated). Thus,

$$\frac{k_n' \cdot W}{2} \cdot (V_{GS} - V_T)^2 = I_D$$, and $I_D = 6.647 \mu A$.

For M2, $V_{GT} = 0.12$, so M2 also is in the saturation region (not velocity saturated). Using the same equation as above and solving for $W/L$ gives $W/L = 8$.

b) Now assume that an ideal current source replaces M2 (Figure 1(b)). The NMOS transistor M1 experiences a shift in $V_T$ due to the backgate effect. Find $V_T$ as a function of $V_o$ for $V_o$ ranging from 0 to 2.5V with 0.5V intervals. Plot $V_T$ vs. $V_o$.

**Solution**

The threshold voltage equation provides the relation that we need:

$$V_T = V_{T0} + \gamma \cdot (\sqrt{2 \Phi_F} + V_{SB} - \sqrt{2 \Phi_F}) = V_{T0} + \gamma \cdot (\sqrt{2 \Phi_F} + V_o - \sqrt{2 \Phi_F})$$

See the graph at the end of this problem.

c) Plot $V_o$ vs. $V_i$ as $V_o$ varies from 0 to 2.5V with 0.5 V intervals. Plot two curves: one neglecting the backgate effect and one accounting for it. How does the backgate effect influence the operation of the level converter?

At $V_o$(with backgate effect) = 2.5V, find $V_o$(ideal) and thus determine the maximum error introduced by the backgate effect.

**Solution**

To plot $V_o$ versus $V_i$ we need to relate $V_o$ to $V_i$. We can do this by solving the current equation (M1 should remain in the same region to first order because $V_{GT}$ will remain roughly constant to maintain the correct drain current) for $V_i$:

$$V_i = V_o + V_T + \frac{2I_D}{\sqrt{k_n' \cdot W}}$$

The maximum error occurs at the highest $V_{SB}$. At $V_o = 2.5$, the error is $3.4944 - 3.1 = 0.3944$ V.
Problem 3: Velocity Saturation

This problem explores the behavior of short-channel devices. For the HSPICE simulations of this problem you will use the 0.18\(\mu\) model parameters. Use the HSPICE model parameters which can be found in “log018_1.l”

a) Using HSPICE plot \(I_D\) versus \(V_{DS}\) for the transistor of the following figure, with \(V_{GS}\) (0.6V, 0.8V, 1V, 1.2V, 1.4V, 1.6V, 1.8V) as a parameter. Comment on the dependence of \(I_D\) with respect to \(V_{GS}\).

**Figure 2:** Short channel Transistor.

\[ V_d \]
\[ V_g \]
\[ V_s \]

**Solution**

The \(I_D\) plots are shown in the next graph.
It is clear from the curves that, for the short channel device, there is a linear dependence of the saturation current with respect to $V_{GS}$.

b) Calculate the effective resistance for a high to low transition, using the method described in slide 44 (Handout 2).

**Solution**

We can use the following expression:

$$ R_{eff} = \frac{1}{2} \left( \frac{V_{DS}}{I_D} \right) v_{DS} = V_{DD} + \left( \frac{V_{DS}}{I_D} \right) v_{DS} = V_{DD}/2 $$
We can find the values of the drain current from the plot. So

\[
R_{\text{eff}} = \frac{1}{2} \left( \frac{1.8}{0.3481 \cdot 10^{-3}} + \frac{0.9}{0.3254 \cdot 10^{-3}} \right) = 4 \text{ } \Omega
\]

c) Consider two CMOS inverters with \( (W_1/L_1)_n = (2.88\mu/1.44\mu) \), \( (W_1/L_1)_p = (5.76\mu/1.44\mu) \) and \( (W_2/L_2)_n = (0.36\mu/0.18\mu) \), \( (W_2/L_2)_p = (0.72\mu/0.18\mu) \). Assume \( V_{\text{DD}} = 1.8 \text{ } \text{V} \) and the output of the inverter is loaded by \( C_L = 100\text{fF} \) capacitance. Calculate the propagation delay \( t_p \) and check the answers with HSPICE.

**Solution**

The propagation delay \( t_p \) is the average of \( t_{pHL} \) and \( t_{pLH} \). We can use the next equations to calculate the rise and fall times for the two inverters.

\[
t_{pHL} = 0.69 R_{eqHL} C_L \quad \text{and} \quad t_{pLH} = 0.69 R_{eqLH} C_L
\]

**Inverter 1**

for a high to low transition (we assume that the PMOS is off):

\[
R(V_{DS} = 1.8V) = 1.8V/0.339m = 5.3K\Omega \quad \text{and} \quad R(V_{DS} = 0.9V) = 0.9V/0.319m = 2.8K\Omega
\]

\[
R_{eq} = \frac{1}{2}(5.3K + 2.8K) = 4.05K\Omega
\]

\[
t_{pHL} = 0.69(4.05K)(100f) = 0.28\text{ns}
\]

for a low to high transition (we assume that the NMOS is off):

\[
R(V_{DS} = -1.8) = -1.8\text{V} / 0.162m = 11.1K\Omega \quad \text{and} \quad R(V_{DS} = -0.9V) = -0.9\text{V}/-0.150m = 6.0K\Omega
\]

\[
R_{eq} = \frac{1}{2}(10.5K + 5.7K) = 8.6K\Omega
\]

\[
t_{pLH} = 0.69(8.1K)(100f) = 0.59\text{ns}
\]

So, \( t_{p1} = \frac{1}{2}(t_{pHL} + t_{pLH}) = 0.435\text{ns} \)

**Inverter 2**

for a high to low transition (we assume that the PMOS is off):

\[
R(V_{DS} = 1.8V) = 1.8V/0.254m = 7.1K\Omega \quad \text{and} \quad R(V_{DS} = 0.9V) = (0.9V)/0.237m = 3.8K\Omega
\]

\[
R_{eq} = \frac{1}{2}(7.1K + 3.8K) = 5.45K\Omega
\]

\[
t_{pHL} = 0.69(5.45K)(100f) = 0.38\text{ns}
\]
for a low to high transition (we assume that the NMOS is off):
\[ R(V_{DS} = -1.8V) = -1.8/0.172m = 10.5K\Omega \text{ and } R(V_{DS} = -0.9V) = -0.9/0.147m = 6.4K\Omega \]

\[ R_{eq} = \frac{1}{2}(6.4K + 10.5K) = 8.5K\Omega \]

\[ t_{pLH} = 0.69(7.9K\Omega)(100f) = 0.58ns \]

So, \[ t_{p2} = \frac{1}{2}(t_{pHL} + t_{pLH}) = 0.48ns \]

The HSPICE simulation gives for the propagation delay:
\[ t_{p1} = \frac{0.45n + 0.8n}{2} = 0.625ns \text{ and } t_{p2} = \frac{0.39 + 0.59n}{2} = 0.49ns \]

Comment.

Hspice simulations give different results than the hand calculations, because there are some second order effects that affect the performance of the devices. If you perform a transient analysis, you will see that in the case of the long channel inverter, there is an overshoot(undershoot) when the new input data arrives. That’s because of clock feedthrough (gate-to-drain capacitive coupling - Chapter 6). The long channel inverter experiences this more intensively, because of the larger sizes of the transistors.

If you make the output load capacitance fairly large then this effect won’t be so obvious, and the inverter with the long channel devices will be faster as expected.

This is shown in the next figure.

The difference for the two transitions, comes from the fact that the for the low-to-high transition the currents for the two inverters are almost the same..

d) Repeat part c) sweeping the supply voltage \( V_{DD} \) from 0.4V to 1.8V (sweep step 0.2V). Plot the propa-
gation delay $t_p$ versus the supply voltage $V_{DD}$ in the same graph. Comment on the results.

Solution

The next table summarizes the propagation delays for the different supply voltages

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>$t_{P\text{inv}1}$ (ns)</th>
<th>$t_{P\text{inv}2}$ (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0.6</td>
<td>9.8</td>
<td>7.7</td>
</tr>
<tr>
<td>0.8</td>
<td>2.9</td>
<td>1.9</td>
</tr>
<tr>
<td>1</td>
<td>1.6</td>
<td>1.1</td>
</tr>
<tr>
<td>1.2</td>
<td>1.1</td>
<td>0.8</td>
</tr>
<tr>
<td>1.4</td>
<td>0.9</td>
<td>0.6</td>
</tr>
<tr>
<td>1.6</td>
<td>0.7</td>
<td>0.5</td>
</tr>
<tr>
<td>1.8</td>
<td>0.6</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Table 2: Propagation Delays for the two inverters

The plot is shown in the next figure.

Comments

We see that the curve for the short channel device flattens (~1.4 V), since $I_D$ is linear with respect to $V_{GS}$.

Problem 4: Voltage transfer characteristics, Noise Margins

The next figure shows an all NMOS inverter.
a) Calculate $V_{OH}$, $V_{OL}$, $V_M$ for the inverter.

\[ V_{DD} = 2.5V \]

\[ M_2 \quad \text{W/L=0.375/0.25} \]

\[ V_{OUT} \]

\[ M_1 \quad \text{W/L=0.75/0.25} \]

\[ V_{IN} \]

\[ A \]

**Figure 3:** Two Inverter Implementations

Solution:

$V_{OH}$: We calculate $V_{OH}$, when $M_1$ is off. The threshold for $M_2$ is:

\[ V_T = V_{T0} + \gamma \cdot (\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \]

$V_{SB} = V_{OUT}$ and $M_2$ will be off when: $V_{GS} - V_T = V_{DD} - V_{OUT} - V_T$, or:

\[ V_{DD} - V_{OUT} = 2.5 - V_{OUT} - 0.43 + 0.4 \cdot (\sqrt{0.6 + V_{OUT}} - \sqrt{0.6}) = 0 \]

We get $V_{OUT} = V_{OH} = 1.765V$.

$V_{OL}$: To calculate $V_{OL}$, we set $V_{IN} = V_{DD} = 2.5V$.

We expect $V_{OUT}$ to be low, so we can make the assumption that $M_2$ will be velocity saturated and $M_1$ will be in the linear region.

For $M_2$: 

\[ I_{D2} = k'_n \cdot \frac{W}{L_2} \cdot \left( (V_{GS} - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda V_{DS}) \]

Setting $I_{D1} = I_{D2}$, we get an equation and we solve for $V_{OUT}$.

We get: $V_{OUT} = V_{OL} = 0.263V$, so our assumption holds. We have input 2.5 V instead of $V_{OH}$, an assumption that is often used. If we instead put $V_{OH}$ at the input, $V_{OL} = 0.38V$ and full credit was given for either solution.

$V_M$: To calculate $V_M$ we set $V_M = V_{IN} = V_{OUT}$.

Assuming that both transistors are velocity saturated, then we have the next pair of equations:
\[ I_{D1} = k' \frac{W_1}{L_1} \cdot \left( (V_M - V_{T0}) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda V_M) \text{ and} \]

\[ I_{D2} = k' \frac{W_2}{L_2} \cdot \left( (V_{DD} - V_M - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda (V_{DD} - V_M)) \]

Setting \( I_{D1} = I_{D2} \), we get for \( V_M = 1.01 \text{ V} \)

b) Use HSPICE to obtain the VTC.

Solution

The VTC is shown below.

\[ \text{c) Calculate } V_{IH}, V_{IL}, \text{ and the noise margin and comment on the results. How can you increase the noise margins and reduce the undefined region?} \]

Solution

Circuit 1

\[ V_{IL} = 0.5\text{ V}, V_{IH} = 1.35\text{ V} \]

\[ \text{NM}_{H} = V_{OH} - V_{IH} = 1.765 - 1.35 = 0.42\text{ V}, \text{NM}_{L} = V_{IL} - V_{OL} = 0.5 - 0.26 = 0.24\text{ V} \]

We can increase the noise margins by moving \( V_M \) closer to the middle of the output voltage swing. Some of you pointed out that the VOH/VOL obtained from HSPICE does not match the value in the hand calculation. This is because, due to diode and leakage currents, the output actually rises higher than \( V_T \) in order to reach DC steady state and match all the tiny leakage currents. (These are second order effects not modeled by the assumption that \( V_{out} \) should rise to \( V_{DD}-V_{T} \)).

d) Comment on the differences in the VTCs, robustness and regeneration between this inverter and a stan-
dard CMOS inverter.

Solution

It is clear from the two VTCs, that a CMOS inverter is more robust, since the low and high noise margins are higher than the first inverter. Also the regeneration in the second inverter is greater since it provides rail to rail output and the gain of the inverter is much greater.

Problem 5: Inverter Gain and Regions of Operation

Figure 0.1 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at $V_M$. The intersection of this line with the $V_{OH}$ and the $V_{OL}$ lines defines $V_{IH}$ and $V_{IL}$.

a) The noise margins of a CMOS inverter are highly dependent on the sizing ratio, $r=k_p/k_n$, of the NMOS and PMOS transistors. What ratio $r$ would be required to achieve equal noise margins if the thresholds of NMOS and PMOS were equal and channel length modulation were ignored? Now use HSPICE and the 0.25µ process file to test your theory. For your simulation, use $W_n=1.0$ um so that $W_p$ will just be equal to $r*(NMOS\ mobility/PMOS\ mobility)$. If there is a discrepancy in the two results you obtain, suggest some possible explanations.

Solution

The TSMC 0.25µm models were used for simulation and the threshold voltages of NMOS and PMOS devices are nearly equal in this process. A value near $r=1$ should result in equal noise margins, since the transistors will be closely matched. HSPICE showed that the resulting noise margins for this sizing were $N_{MH}=0.97$ V and $N_{ML}=1.1$ V. The mismatch is due to the fact that the PMOS threshold voltage is actually slightly lower, so the PMOS is stronger and the upper noise margin is reduced. In addition, the NMOS velocity saturates at a lower voltage, further increasing the relative strength of the PMOS when both devices are in velocity saturation. The actual value that results in equal noise margins is $r=0.83$.

b) Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for $NM_H$ and $NM_L$ in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at $V_M$. For what range of $r$ is this assumption valid? What is the resulting range of $V_M$?

Solution

Using the equations for finding the region of operation, it can be shown that the PMOS and NMOS are both velocity saturated only while the switching threshold is between 1.06 V and 1.10 V. Since this range may be considered inclusive, we can assume that both devices are velocity saturated and set the currents equal with $V_{IN}=V_{OUT}-V_M$ to find $k_p/k_n$. Depending on the assumptions we make when we find $r$, there are a range of possible results. Some people used the definition of $r$ that includes variation in VDSAT for NMOS and PMOS, some included the effect of channel length modulation, and other combinations of the above considerations. Since the problem was slightly ambiguous on this topic full credit will be given for any of the answers.

The equation below gives $k_p/k_n$ in terms of known circuit parameters. Leaving out channel-length modulation results in slightly different numbers. Then, whether $r$ is defined as $k_p/k_n$ or $(k_p*V_{dsatp})/(k_n*V_{dsatn})$ produces two different results due to the different definitions.
Some of you, however, used the equation for \( r \) given on page 186, equation 5.6 of the text. Although you coincidentally got the same numbers as one of the results above, this method isn’t valid because this equation is for the case when both NMOS and PMOS are saturated, NOT velocity saturated.

This result can be checked by sizing the devices accordingly and testing the resulting \( V_M \) in HSPICE. The result gives a range of 1.04 V to 1.09 V. This makes sense, because the NMOS must be much stronger than the PMOS to achieve a switching threshold near 1 V.

c) Derive expressions for the inverter gain at \( V_M \) for the cases when the sizing ratio is just above and just below the limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS for each case? Consider the effect of channel-length modulation by using the following expression for the small-signal resistance in the saturation region:

\[
\frac{k_p}{k_n} = \frac{v_{dsat} \left[ v_{m} - v_{tn} - \frac{v_{dsat}}{2} \right] \left[ 1 + \lambda v_m \right]}{v_{dsat} \left[ v_{m} - v_{dd} - \frac{v_{dsat}}{2} \right] \left[ 1 + \lambda (v_m - v_{dd}) \right]}
\]

### Table of ‘\( r \)’ Ranges

<table>
<thead>
<tr>
<th>Lambda Included</th>
<th>VDSAT Included</th>
<th>VDSAT Not Included</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.54-0.65</td>
<td>0.34-0.41</td>
</tr>
<tr>
<td>Lambda Not Included</td>
<td>0.58-0.71</td>
<td>0.37-0.45</td>
</tr>
</tbody>
</table>

**Solution**

When \( V' \) is slightly smaller than 1.06 V, the PMOS is velocity saturated and the NMOS is saturated. Section 5.3.2 of the text shows this derivation for the case when both devices are velocity saturated. These derivations can be completed by substituting the correct current equations and using the same method. The results are as follows:

For the case when the NMOS is saturated and the PMOS is velocity saturated:

\[
\frac{dV_{out}}{dV_{in}} = \frac{k_p (V_{in} - V_{tn}) (1 + \lambda V_{out}) + k_p v_{DSATP} (1 + \lambda V_{out} - V_{DD})}{k_n k_p (V_{in} - V_{tn})^2 + k_p v_{DSATP} \lambda_p (V_{in} - V_{DD} - V_{tp} - V_{DSATP}/2)}
\]
Dropping the second order terms in the numerator, substituting $V_m$ for $V_{in}$, and simplifying the denominator leads to the following expression for the gain:

$$\frac{dV_{out}}{dV_{in}} = \frac{k_n (V_m - V_{in}) + k_p V_{DSATP}}{I_D(V_m)(\lambda_n - \lambda_p)}$$

**Problem 6: Static CMOS Inverter**

For this problem use scalable CMOS design rules and assume:

$V_{DD} = 2.5V$, $W_p/L = 1.25/0.25$, $W_N/L = 0.375/0.25$, $L_{eff} = 0.25\mu m$ (i.e. $x_d = 0\mu m$), $C_{L} = C_{inv-gate}$, $k_n' = 115\mu A/V^2$, $k_p' = -30\mu A/V^2$, $V_{tn0} = |V_{tp0}| = 0.4V$, $\gamma = 0.4$, and $t_{ox} = 58A$. Use the Hspice model parameters for parasitic capacitance given below (i.e. $C_{gdo}$, $C_j$, $C_{jsw}$), and assume that $V_{SB} = 0V$ for all problems except part (e).

Use the following values for $V_{tn0}$, $V_{tp0}$, and $t_{ox}$:

- $V_{tn0} = |V_{tp0}| = 0.4V$
- $\gamma = 0.4$
- $t_{ox} = 58A$

**Diagram:**

![CMOS Inverter with Capacitive Load](image)

*Figure 4: CMOS inverter with capacitive load.*

### Parasitic Capacitance Parameters (F/m)###

**NMOS**
- $C_{GDO} = 3.11 \times 10^{-10}$
- $C_{GSO} = 3.11 \times 10^{-10}$
- $C_J = 2.02 \times 10^{-3}$
- $C_{JSW} = 2.75 \times 10^{-10}$

**PMOS**
- $C_{GDO} = 2.68 \times 10^{-10}$
- $C_{GSO} = 2.68 \times 10^{-10}$
- $C_J = 1.93 \times 10^{-3}$
- $C_{JSW} = 2.23 \times 10^{-10}$

a) What is the $V_m$ for this inverter?

**Solution**

Assume that $V_m$ is around midrail (1.25V). That means that the NMOS is velocity saturated and the PMOS is saturated. To find $V_m$, we set the sum of the currents at $V_{out}$ equal to 0 using the correct equation for each device:

$$k_n \cdot V_{DSATn} \left( V_M - V_{tn} - \frac{V_{DSATn}}{2} \right) + k_p \cdot 0.5 \cdot (V_M - V_{DD} - V_{tp})^2 = 0$$

Plug in numbers:
172.5 \cdot 0.6 \cdot (V_M - 0.4 - 0.315) + (-150) \cdot 0.5 \cdot (V_M - 2.5 - (-0.4))^2 = 0

103.5V_M - 74 - (-75 \cdot (V_M^2 - 4.2V_M + 4.41)) = 0.

Solving this quadratic gives \(V_M = 1.245\) V.

b) What is the effective load capacitance \(C_{Leff}\) of this inverter? (include parasitic capacitance, refer to notes for \(K_{eq}\) and \(m\).) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, \(\lambda = 0.125\) \(\mu\)m, and the source/drain extensions are 5\(\lambda\) for the PMOS; for the NMOS the source/drain contact regions are 5\(\lambda\)x5\(\lambda\).

**Solution**

The calculation of the lumped load capacitance follows the format presented in the lecture notes. The only difference is the dimensions of the devices.

\[C_{Leff} = C_L + C_{parasitic} = C_{g3} + C_{g4} + C_{db1} + C_{gd1} + C_{gd2} - \]

\[C_{g3} = (C_{GDON} + C_{GSOn})W_n + C_{ox}W_nL = 2(3.11 \times 10^{-10})(0.375 \times 10^{-6}) + 6 \times 15(0.375)(0.25) = 0.796fF\]

\[C_{g4} = (C_{GDOP} + C_{GSOp})W_p + C_{ox}W_pL = 2(2.68 \times 10^{-10})(1.25 \times 10^{-6}) + 6 \times 15(1.25)(0.25) = 2.545fF\]

\[C_{db1} = K_{eqn}(AD_n)C_j + K_{eqswn}(PD_n)C_{jsw}.\text{ Need to do this calculation for both transitions and average the results. The Keq values are already calculated in the notes.}\]

\[AD_n = AS_n = 1.25\mu m \times 0.625\mu m = 0.78125\mu m^2\text{ and } AD_p = AS_p = 0.125\mu m \times 0.375 + 0.625^2 = 0.4375\mu m^2.\]

\[PD_n = PS_n = 2 \times 0.625\mu m + 1.25\mu m = 2.5\mu m\text{ and } PD_p = PS_p = 5 \times 0.125\mu m \times 3 + (2 + 1 + 1) \times 0.125\mu m = 2.375\mu m.\]

\[(0.57 \times 0.4375 \times 2 + 0.61 \times 2.375 \times 0.28) = 0.904fF\text{ for HL transition}\]

\[(0.79 \times 0.4375 \times 2 + 0.81 \times 2.375 \times 0.28) = 1.23fF\text{ for LH. Average } C_{db1} = 1.067fF.\]

\[C_{db2} = K_{eqp}(AD_p)C_j + K_{eqswp}(PD_p)C_{jsw.}\]

\[(0.79 \times 0.78125 \times 1.9 + 0.86 \times 2.5 \times 0.22) = 1.65fF\text{ for HL transition}\]

\[(0.59 \times 0.78125 \times 1.9 + 0.7 \times 2.5 \times 0.22) = 1.26fF\text{ for LH. Average } C_{db2} = 1.455fF.\]

\[C_{gd1} = 2C_{GDON}W_n = 2 \times 3.11 \times 10^{-10} \times 0.375 \times 10^{-6} = 0.233fF.\]

\[C_{gd2} = 2C_{GDOP}W_p = 2 \times 2.68 \times 10^{-10} \times 1.25 \times 10^{-6} = 0.67fF.\]

\[C_L = \text{sum} = 6.767fF.\text{ Note - since the problem states that } x_d = 0,\text{ it is ok if you neglected the last two parasitic capacitances. We intended for them to be included, though.}\]

c) Calculate \(t_{PHL}, t_{P LH}\) assuming the result of (b) is ‘\(C_{Leff} = 6.5fF\)’. (Assume ideal step input, i.e. \(t_{rise} = t_{fall} = 0\). Do this part by computing the average current used to charge/discharge \(C_{Leff})\)

**Solution**

We can estimate the propagation delay using the approximation \(\Delta t = \Delta Q/I\), where \(\Delta Q = C_{Leff}V_{DD}\) and \(I\) is
the average current used to charge/discharge $C_{\text{eff}}$. During the high-to-low transition $C_{\text{eff}}$ is discharged through the NMOS transistor so $I = I_{\text{avg}N}$. During the low-to-high transition $C_{\text{eff}}$ is charged through the PMOS transistor so $I = I_{\text{avg}P}$. In summary

$$I_{\text{delay}} = \frac{V_{DD} \cdot C_{\text{eff}}}{2 \cdot I_{\text{avg}}}$$

where

$$I_{\text{avg}N} = \frac{I_{ds}(V_o = 0) + I_{ds}(V_o = \frac{V_{DD}}{2})}{2}, I_{\text{avg}P} = \frac{I_{ds}(V_o = V_{DD}) + I_{ds}(V_o = \frac{V_{DD}}{2})}{2}$$

Table 3 shows corresponding values for $I_{\text{avg}N}$, $I_{\text{avg}P}$, $t_{\text{PLH}}$ and $t_{\text{PHL}}$. NOTE- This solution included channel length modulation, but it is ok if your solution did not (see problem assumptions).

d) Find $(W_p/W_n)$ such that $t_{\text{PHL}} = t_{\text{PLH}}$.

Solution

One way to do this is to solve the current average equations for $W_p/W_n$ after setting the propagation delays equal to one another. A much easier method is to sweep the widths in HSPICE. The HSPICE sim shows that $W_p/W_n = 2.6$ gives equal rise and fall times.

e) Suppose we increase the width of the transistors to reduce the $t_{\text{PHL}}$, $t_{\text{PLH}}$. Do we get a proportional decrease in the delay times? Justify your answer.

Solution

The propagation delays DO NOT decrease in proportion to the widths because of self-loading effects. As the device size increases, its parasitic capacitances increase as well. In this problem, increasing device size increases both average current and $C_{\text{eff}}$.

f) Suppose $V_{SB} = 1V$, what is the value of $V_{\text{tn}}$, $V_{\text{tp}}$, $V_m$? How does this qualitatively affect $C_{\text{eff}}$?

Solution

$$V_{\text{tp}} = V_{\text{tp}0} = -0.4V.$$  

$$V_{\text{tn}} = 0.4 + \gamma \cdot (\sqrt[4]{2\phi_F} + 1 - \sqrt[4]{2\phi_F}) = 0.596 \text{ V}.$$  

Using the equation for part a) and plugging in the new value of $V_{\text{tn}}$ gives: $V_M = 1.35V$

The increased $V_{sb}$ will increase the depletion region and lower the junction capacitance, lowering $C_{\text{eff}}$.

g) Use Magic to create a layout for this inverter. Extract the schematic, including parasitic capacitance, from the layout and use HSPICE to simulate the circuit and measure $t_p$ and the average power for the
following input $V_{in}$: pulse(0 $V_{DD}$ 5n 0.1n 0.1n 9n 20n), as $V_{DD}$ varies from 1V - 2.5V with 0.25V interval. $t_P = (t_{PHL} + t_{PLH}) / 2$. Using this data, plot ‘$t_P$ vs. $V_{DD}$’, and ‘Power vs. $V_{DD}$’.

The extracted layout will include parasitics so you need not manually include AS, AD, PS, PD in your spice deck, but remember to manually add $C_L = 6.5fF$. Set $V_{SB} = 0V$ for this problem. Use the HSPICE model parameters which can be found in “logic025.l”.

Solution

There are many valid layouts for the inverter and you can find an example in the book. For one possible layout, the simulation results are as follows. (The parasitics should be quite similar for any reasonable layout.)

h) Using HSPICE, simulate the circuit for a set of ‘pulse’ inputs with rise and fall times of $t_{in\_rise,\_fall} = 1ns, 2ns, 5ns, 10ns, 20ns$. For each input, measure (1) the rise and fall times $t_{out\_rise}$ and $t_{out\_fall}$ of the inverter output, (2) the total energy lost $E_{total}$, and (3) the energy lost due to short circuit current $E_{short}$. For measuring short circuit power, use the technique discussed in class (slide 96, Handout 2). Use the HSPICE model parameters which can be found in “logic025.l”.

Using this data, prepare a plot of (1) $(t_{out\_rise}+t_{out\_fall})/2$ vs. $t_{in\_rise,\_fall}$, (2) $E_{total}$ vs. $t_{in\_rise,\_fall}$, (3) $E_{short}$ vs. $t_{in\_rise,\_fall}$ and (4) $E_{short}/E_{total}$ vs. $t_{in\_rise,\_fall}$.

Provide simple explanations for:
(i) Why the slope for (1) is less than 1?
(ii) Why $E_{short}$ increases with $t_{in\_rise,\_fall}$?
(iii) Why $E_{total}$ increases with $t_{in\_rise,\_fall}$?

Solution

i) The slope is less than 1 because of the regenerative property of the inverter. The high gain around the
switching point causes the output to change faster than the inputs.

ii) The amount of time for which both devices are on simultaneously increases.

iii) Total energy increases because the short circuit energy begins to dominate, and it increases as the rise/fall time increases.

Plots for Problem 4(h)
Problem Set #1: Updates and Frequently Asked Questions

Notes and Hints:

Problem 2:

- Some of you have asked about the regions of operation of the devices. Ignore the given VDD=2.5V and assume VDD is large enough that M1 does not go into subthreshold or linear operation when Vo is swept to 2.5 V. (You don't even need to know an exact value for this particular problem since lambda=0 - just assume it's large enough.) Given that condition, you know enough about VGT and VDSAT to determine the regions of operation.

Problem 3:

- Assume VDD=1.8 V for the entire problem. (To clarify, this does NOT mean that the drain is always connected to VDD! Think about the appropriate drain voltage for each section of the problem.)
- In part b, don't calculate entirely by hand. Use the I-V curves to find the resistance from the HSPICE simulation.
- For parts b and c you need only to consider the case where vdd=vgs(max)=1.8V. For parts a and d you may want to consider using .DATA and .MEASURE statements to make your work easier.

The .DATA statement has syntax as follows and is used to repeat a particular transition for a set of conditions: (if you have parameterized vd in a statement
.param vd=1.8V)

```
.DATA D1 vd
+ 0.6
+ 0.8
+ 1.0
+ 1.2
+ 1.4
+ 1.6
+ 1.8
```
Then, in your transient analysis: .tran SWEEP DATA=D1 (Where step size and stop time are the values you have chosen. Given this parameterization, the easiest way to find and plot the propagation delays is to use .MEASURE statements. An example of this is: .MEASURE TRAN tdf TRIG V(in) VAL='vd/2' RISE=1 TARG V(out) VAL='vd/2' FALL=1 More documentation on how to use these statements is available in the complete documentation available through the course web page.

Problem 4:

- You will not get the same result for VOH by hand and with HSPICE. The hand calculation is based on the assumption that that M2 will stop charging the output node when the node reaches VDD-VT, (where VT includes body effect). In fact, transistors have non-zero subthreshold current and the final output voltage in the simulation is determined as several second order effects adjust the voltage to make the DC currents sum to zero. So, just use your VTC from part b to answer the questions in part c.

Problem 5:

- As stated, question 5a doesn't really make sense. Please reword 5a as follows: "The noise margins of a CMOS inverter are highly dependent on the sizing ratio, \( r=\frac{k_p}{k_n} \), of the NMOS and PMOS transistors. What ratio \( r \) would be required to achieve equal noise margins if the thresholds of NMOS and PMOS were equal and channel length modulation were ignored? Now use HSPICE and the 0.25u process file to test your theory. For your simulation, use \( W_n=1.0 \) um so that \( W_p \) will just be equal to \( r*(\text{NMOS mobility/PMOS mobility}) \). If there is a discrepancy in the two results you obtain, suggest some possible explanations."
- Some of you have asked about including \( \frac{vdsat_p}{vdsat_n} \) in the \( r \) equation. For this problem only, do just use \( r \) as defined above for part a. You can think of this as the ideal case when threshold voltages, channel length modulation, and saturation voltages are equal for NMOS and PMOS. Since the \( vdsat \) terms are ratioed in this equation leaving out the two terms is equivalent to pretending they’re equal. The explanation section is a good opportunity to discuss which of the prior assumptions might have been primarily responsible for causing any difference between your calculated \( r \) in the above expression and the value you actually get from simulation.

Problem 6:

- For the parts of the problem involving \( K_{eq} \), find the \( C \) values for both transistions and average the results to get the effective capacitance.
For these problems you should use the parameters for the 0.25 technology (given in the text) unless otherwise specified for a particular problem.

Problem 1: Subthreshold Inverter Operation

In circuit applications where extremely low power consumption is essential and high speed operation is not required, subthreshold logic may provide an ideal solution. This problem will explore how far the supply voltage may be lowered before a CMOS inverter fails. For the entire problem, assume that the both devices are minimum length and that the NMOS device has a width of 0.44 um. Failure is defined as the point where an input swing of 0 to VDD produces an output swing less than 10% to 90% of VDD. For this problem use the 0.18 micron technology file which is located in “/mit/6.374/models/log018_1.l”. (Research by Alice Wang)

a) Consider the case where the input to the inverter is 0 V. Will the output voltage remain equal to the supply voltage as the supply voltage is lowered to arbitrarily low values? If not, explain what will happen and why. Would using a wider PMOS device increase or decrease the minimum possible supply voltage? Which process corner (TT, FF, SS, SF, or FS) will be the worst case and why? (Variable process conditions may result in a case where the NMOS and PMOS devices have modified mobilities. TT is the case where both devices are typical, SF has slow NMOS and fast PMOS, etc...)

Solution

When the input is 0 V, Vgs for the NMOS device is 0 V and Vgs for the PMOS is -VDD. For typical supply voltages, the current through the PMOS in this case dominates and the output is pulled to VDD. As VDD falls to lower voltages, eventually pushing the PMOS into subthreshold the currents will eventually begin to approach comparable levels and the simple CMOS inverter will become a ratioed circuit. Using a wider PMOS would decrease the minimum possible supply voltage since this would increase the strength of the PMOS relative to the NMOS and allow the CMOS inverter to overpull the NMOS for lower supply voltages. FS would be the worst case process corner, since the PMOS is weakened in comparison to the NMOS and looses some ability to pull up the output node. So, for a given supply voltage there is a minimum width requirement on the PMOS to maintain proper operation and the minimum size is largest for the FS corner.

b) Consider the case where the input to the inverter is VDD. Would using a wider PMOS increase or decrease the minimum supply voltage in this case? Which process corner will be the worst case and why?

Solution

In this case, Vgs for the PMOS is 0 V and Vgs for the NMOS is lowered with supply voltage. Using a wider
PMOS would increase the minimum supply voltage since the PMOS would be stronger and have more leakage current to pull the output up from its desired value of 0 V. The worst case corner would be SF since this would also increase the output voltage for a given supply voltage. So for a given supply voltage, there is a maximum width for the PMOS to maintain proper operation and the maximum width is smallest for the SF corner. Comparing the results for parts a and b, it is clear that since one case requires large PMOS and one case requires small PMOS there must be an optimum PMOS size to operate at the lowest possible supply voltage.

c) Now, use HSPICE to simulate the inverter and find the lowest possible supply voltage. Complete one simulation for each input value using the process corners you chose in parts a and b. Use a .DATA statement to vary the width of the PMOS device across the set \{0.5u, 1u, 1.5u, 2u, 4u, 8u, 10u, 15u, 30u, 45u, 60u\} and sweep VDD from 100mV to 400 mV. Then, using the expressions function in AWaves, plot the ratio of V(out)/VDD. The points where the ratio crosses 0.1 and 0.9 are the failure points. Create a table with three columns containing: PMOS width, minimum supply voltage for the case where the input voltage equals 0, and minimum supply voltage for the case where the input voltage equals VDD.

<table>
<thead>
<tr>
<th>PMOS Width</th>
<th>0.5u</th>
<th>1.0u</th>
<th>1.5u</th>
<th>2u</th>
<th>4u</th>
<th>8u</th>
<th>10u</th>
<th>15u</th>
<th>30u</th>
<th>45u</th>
<th>60u</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. VDD (Vin=VDD)</td>
<td>118m</td>
<td>120m</td>
<td>134m</td>
<td>150m</td>
<td>184m</td>
<td>213m</td>
<td>221m</td>
<td>235m</td>
<td>260m</td>
<td>274m</td>
<td>284m</td>
</tr>
<tr>
<td>Min. VDD (Vin=0)</td>
<td>275m</td>
<td>273m</td>
<td>256m</td>
<td>238m</td>
<td>201m</td>
<td>172m</td>
<td>163m</td>
<td>150m</td>
<td>128m</td>
<td>115m</td>
<td>107m</td>
</tr>
</tbody>
</table>

The minimum supply voltage is about 190 mV and the PMOS must be about 5 um.

d) Now use your favorite graphing program (Matlab, Excel, etc...) to create a graphical representation for the functional region of operation. On a single graph, plot both cases of (minimum supply voltage, PMOS width) and indicate the region where both conditions are met. What is the lowest possible supply voltage that meets both conditions? What must the PMOS width be to operate at this supply voltage? The minimum supply voltage is about 190 mV and the PMOS must be about 5 um.
Problem 2: CMOS Logic

Consider the following CMOS logic circuits:

![Circuit A](image1.png)

![Circuit B](image2.png)

Figure 0.1: Two static CMOS gates

a) Do the two circuits in Figure 0.1 implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

**Solution**

Yes, they implement the same logic function: \( F = (A \cdot B \cdot C \cdot D) + E \) = \( (A + B + C + D) \cdot E \)

b) Assuming we can ignore all second-order effects, do these two circuits have the same output resistances when driven with the same input patterns?

**Solution**

Yes, they do. The pull down networks are identical and the pull up network can be found by inspection to have the same resistances given the same input pattern.

c) Assume the transistors have been sized to give a worst case output resistance of 13 kΩ for the worst-case input pattern. What input patterns \((A-E)\) give the lowest output resistance when the output is low? What is the value of that resistance?

**Solution**

The lowest output resistance is obtained when all inputs \((A, B, C, D\) and \(E)\) are equal to 1. In that case, the output resistance is the parallel of the resistance of a NMOS of width 1, with a series of four equal nMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, 13 kΩ. Then the output resistance, in this case, is half this value, 6.5 kΩ.

d) What input patterns \((A-E)\) give the lowest output resistance when the output is high? What is the value of that resistance?
Solution

The lowest output resistance is obtained when all inputs are equal to zero. Each of the PMOS have the same width, so all of them have the same resistance. The worst case resistance happens when only one of the inputs (A, B, C or D) is equal to 0 while all the rest are equal to 1. The output resistance in that case is the series of the resistance of two of the PMOS and it is equal to 13 kΩ. Then, each of the pMOS has an output resistance equal to 6.5 kΩ. The output resistance is equal to the series of one of these resistance with the parallel of four of the same resistances. Then, the minimum output resistance is 6.5 kΩ + 6.5 kΩ /4 = 8.125 kΩ.

e) Neglecting parasitics and assuming a load capacitance of 100 fF, find the best case and worst case t_{phl} and t_{plh}.

Solution

We can use the RC time constant method of \( t = 0.69 \times R_{eq} \times C_L \). For the worst case, \( R = 13 \) K for both pull-up and pull-down and the \( t_{phl} \) and \( t_{plh} \) are both equal to 0.9 ns. For the best case \( tphl \) we know that \( R = 6.5 \) K so \( t_{phl} = 0.45 \) ns. For the best case \( t_{plh} \) we know that \( R = 8.125 \) K so \( t_{plh} = 0.56 \) ns.

f) Now consider a few second order effects on the propagation delays. Which circuit is optimized for the case when it is known a priori that E will be the last input to arrive and why? How will body effect influence the performance of Circuit A vs. Circuit B?

Solution

Circuit B is optimized for the case when ‘E’ will arrive last. The only difference between the two circuits is the pull up network. The nodes between (ABCD) and (E) can use the time before E arrives to charge up to VDD therefore reducing the time required for the overall circuit to charge after E does arrive. Circuit B is also preferable due to the lower influence of body effect. All four parallel devices in Circuit A may experience an increase in threshold voltage and consequent decrease in drive strength due to body effect.

g) For parts g and h, consider only Circuit B. Each intermediate node has some parasitic capacitance that must be charged and discharged at each transition. Therefore, the propagation delay is a function of both the initial voltage conditions on the internal nodes and the inputs. The initial voltage conditions, however, are determined by the previous inputs. Which set of previous and current inputs will cause the slowest \( t_{phl} \)? Which will cause the slowest \( t_{plh} \)?

Solution

For the worst case low-to-high output transition, all internal caps should initially be discharged to ground which gives a worst case previous input of \( [ABCDE] = [11110] \). Then, the following input should leave all of those capacitances exposed to the output node so \( [ABCDE] = [11100] \). For the high-to-low transition, we should have \( [ABCDE] = [11100] \) as the previous input to charge up the internal nodes, then \( [ABCDE] = [11110] \) to discharge through a single path only.

h) Let all devices be minimum length and set the widths according to the relative scale in the diagram with \( 1 = 0.375 \) um, specify your source and drain areas and perimiters, and include an additional 10 fF load. Use Nanosim to verify functionality by creating an input file which tests the following set of inputs \( [ABCDE] = [00000, 00001, 11110, 11100, 11111] \). Verify that your simulated output values match the expected logic function. Submit your Nanosim output file.

Solution
Problem 3: Pseudo-NMOS Logic

Consider the circuit of Figure 0.2.

a) What is the output voltage if only one input is high? If all four inputs are high?

Solution

\[ I_D = k' \cdot \frac{W}{L} \left( V_{GT} \cdot V_{min} - \frac{V_{min}}{2} \right)^2 \cdot (1 + \lambda \cdot V_{DS}) \]

Consider a case when one input is high: A = \( V_{DD} \) and B = C = D = 0 V. Assume that \( V_{out} \) is small enough that \( V_{min} = V_{DSAT} \) for the PMOS device, and \( V_{min} = V_{DS} = V_{out} \) for the NMOS devices. Solve for \( V_{out} \) by setting the drain currents in the PMOS and NMOS equal to each other, \( |I_{DP}| = |I_{DN}| \), where the drain currents are functions of \( V_{out}, V_{DD}, \) and the device parameters.

\( V_{out} = 102 \text{ mV}, \) and \( I_D = 35.7 \mu A. \)

Now verify that the assumptions for \( V_{min} \) are correct. For the PMOS: \( V_{DS} = -2.3 \) V, \( V_{DSAT} = -1 \) V, \( V_{GT} = -2.1 \) V, therefore \( V_{min} = V_{DSAT}. \) For the NMOS: \( V_{DS} = 102\text{mV}, V_{DSAT} = 630\text{mV}, V_{GT} = 2.07 \) V, therefore \( V_{min} = V_{DS}. \)

Consider the case when all inputs are high: A = B = C = D = \( V_{DD}. \) For these hand calculations, this is numerically equivalent to a circuit with a single NMOS device with W/L = 4*1.5 and its gate tied to \( V_{DD}. \) Now, the analysis used above for the case when one device is on can be reused, replacing W/L of the NMOS with 6, and using the same assumptions for \( V_{min} \).

\( V_{out} = 25 \text{ mV}, \) and \( I_D = 35.9 \mu A. \) The assumptions for \( V_{min} \) are correct.

b) What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

Solution

Notice in part a) that the drain current in the PMOS is 35.7 \( \mu A \) with one NMOS on and 35.9 \( \mu A \) with four NMOS devices on. The current in the PMOS can be approximated as 35.8 \( \mu A \) when any number of NMOS devices are on and 0 \( \mu A \) when all four are off. The probability that all four NMOS devices are off is \((1-\rho)^4\) where \( \rho \) is the probability an input is high. Therefore,

\[ P_{AVG} = P_{OFF} \cdot (1-\rho)^4 + P_{ON} \cdot [1 - (1-\rho)^4] \]

where \( P_{OFF} = 0 \text{ W}, \) and \( P_{ON} = 89.5 \text{ \mu W}. \) \( P_{AVG} = 83.9 \text{ \mu W} \) when \( \rho = 0.5 \) and \( P_{AVG} = 30.7 \text{ \mu W} \) when \( \rho = 0.5. \)

c) Compare your analytically obtained results to a SPICE simulation.

Solution

From SPICE: \( V_{out} = 98.7 \text{ mV}, \) and \( I_D = 38.2 \mu A \) with one NMOS device on and \( V_{out} = 23.5 \text{ mV}, \) and \( I_D = \)
38.3 µA with all NMOS devices on

Problem 4: Pass Transistor Logic and Level Restoration

Consider the circuit of Figure 0.3. Assume the inverter switches ideally at \( V_{DD}/2 \), neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

a) What is the logic function performed by this circuit?

Solution

The circuit is a NAND gate.

b) Explain why this circuit has non-zero static dissipation.

Solution

When \( A=B=V_{DD} \), the voltage at node \( x \) is \( V_X = V_{DD} - V_{IN} \). This causes static power dissipation at the inverter the pass transistor network is driving.

c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

Solution

(See diagram with transistor sizes calculated.)
The modified circuit is shown in the next figure:

![Circuit Diagram](image)

The size of $M_r$ should be chosen so that when one of the inputs $A$ or $B$ equals 0, either $M_{n1}$ or $M_{n2}$, would be able to pull node $X$ to $V_{DD}/2$ or less.

d) Implement the same circuit using transmission gates.

**Solution**

The circuit is shown below:

![Transmission Gate Circuit](image)

e) Replace the pass-transistor network in Figure 0.3 with a pass transistor network that computes the following function $x = ABC$ at the node $x$. Assume you have the true and complementary versions of the three inputs $A$, $B$, and $C$.

**Solution**

One possible implementation is shown:
Problem 5: Device Modeling - DIBL

The standard equation for modeling subthreshold leakage current given in the notes is

\[ I_d = I_o \cdot e^{\frac{V_{GS} - V_T}{nV_{th}} \cdot \left( 1 - e^{\frac{-V_{DS}}{V_{th}}} \right)} . \]

This equation does not account for higher order effects like DIBL. The following BSIM equation adds the DIBL effect to the model:

\[ I_d = I_o \cdot e^{\frac{V_{GS} - V_T - (\gamma \cdot V_{SB}) + \eta \cdot V_{DS}}{nV_{th}} \cdot \left( 1 - e^{\frac{-V_{DS}}{V_{th}}} \right)} . \]

Using this new equation, we will produce a model for the subthreshold leakage in the 0.25μm process used in 6.374.

a) Using HSPICE, plot \( I_d \) vs \( V_{GS} \) for a single NMOS device with \( V_D = V_{DD} = 2.5V \) and \( W/L = 0.5\mu m/0.25\mu m \). We are only interested in the subthreshold region, so sweep \( V_{GS} \) over the appropriate range.

Using HSPICE, plot \( I_d \) vs \( V_{DS} \) for \( V_{GS} = 0V \) over the full range of \( V_{DS} \). Plot the current on a log scale for both plots.

You will need to extract the points along these curves to use in your favorite analysis program (ie Matlab) for the rest of this problem. The following statement in HSPICE prints a table of the sweeping value and the current through a MOSFET to the HSPICE output stream: .print dc i(Mn1)
b) Using the data from the $I_d$ vs $V_{GS}$ plot, extract a value for $S$, the subthreshold slope, in mV/decade. Plot $S$ as it varies with $V_{GS}$. Over which range of $V_{GS}$ is $S$ likely to be the most accurate for modeling? Plot “instantaneous $n$” as it varies with $S$. Over which range is it likely to be accurate for modeling?

**SOLUTION:**

The slope of the curve in the $I_d$ vs $V_{GS}$ plot is $1/S$. To find $S$, we need to find the slope of the curve and then take its inverse. We cannot calculate the derivative directly because we want $S$ to be in units of mV/decade. Thus we take the log of the current before finding the slope (notice that we can plot the $\log_{10}(I_d)$ vs $V_{GS}$ on a linear scale and get the same shape curve as in the simulation plot above). The following expression then gives the subthreshold slope in mV/decade:

$$S = \frac{\Delta V}{\Delta \log(I_d)}$$

In Matlab, this might look like: $S = \text{delV/diff(log10(Id))}$;

where delV is the voltage step in mV. We can solve for “instantaneous $n$” using $S=nV_{th}\ln(10)$. The plots for $S$ and “instantaneous $n$” appear on the following page. The region of interest is clearly the right side of the graph ($V_{GS}$ about 0.15V and above). The rise in $S$ at low voltages comes from the tail-up of current. This increase in current at low $V_{GS}$ and high $V_{DS}$ results from the GIDL effect (Gate Induced Diode Leakage). For modeling purposes, we will select a value of $S$ and $n$ from the regions of the plots where the slope is more constant.
c) Now we will construct a model for the subthreshold behavior of the FET using the BSIM equation. This model should accurately represent the behavior of the FET that you saw in part a). The BSIM equation still is a reasonably low order model, so do not expect your final result to match the plots precisely - just try for a ballpark match. To develop the model, you need to select three parameters: \( n \), \( I_o \), and \( \eta \). The value for \( n \) should be somewhere in the range that you plotted in b). Select \( I_o \) so that the drain current supplied by the model matches the simulated value at \( V_{GS}=V_{T0} \).

**Hints:** Pick an initial value for \( \eta \) and use it with your estimates for \( n \) and \( I_o \) in the model equation for varying \( V_{DS} \). \( \eta \) controls the slope of the curve versus \( V_{GS} \). Once the slopes are roughly equivalent, use your estimate of \( \eta \) to find the current while sweeping \( V_{GS} \). Select values of \( n \) and \( I_o \) that give a good fit. Now use those values in the other case to refine your choice of \( \eta \). Iterate this process a few times until you are satisfied with the models. It is helpful to convince yourself (by experimentation or from the equation) of the effects of the different parameters on the current. Remember, there is a range of “right” answers to this part of the problem. Also, be glad you don’t do this for a living!

Turn in a plot of \( I_o \) vs \( V_{GS} \) with the real data and the model data on the same plot. Do the same for \( I_o \) vs \( V_{DS} \). What were your values for \( I_o \), \( n \), and \( \eta \)? Comment briefly on what you consider to be a “good” fit using this model for this process (ie - is it more important to get the slope right or the actual values? is it better to overestimate or underestimate the current? etc). Why is your model a good choice?

We selected \( n = 1.55 \), \( \eta = 0.019 \), and \( I_o = 1.0715E-7 \)A. The choice of \( I_o \) causes the subthreshold current to match the simulated value at \( V_{GS}=V_{T0} \) for our choice of \( \eta \) and \( n \). We selected \( n \) such that the difference between the model and the simulation was very small at \( V_{GS}=0 \). This allows our model for varying \( V_{DS} \) to match more closely in magnitude. This approach may not be ideal, however. By matching the magnitude of the current at \( V_{GS}=0 \), we actually do a fairly poor job of matching the slope of the curve vs \( V_{GS} \). If matching the magnitude of the curve vs \( V_{DS} \) is not so important, we could do a better job of matching the slope vs \( V_{GS} \). Also, the choice of \( \eta \) changes the slope of the curve as \( V_{DS} \) varies. Again, different choices of this parameter allow a better match over different regions of the curve. You see that the limitations of this model force some trade-offs in the decision.
Problem 6: DCVSL Gate Design

a) Implement the function \( S = A B C + \overline{A} B \overline{C} + \overline{A} B C + \overline{A} B \overline{C} \) using transmission gate logic. What function does this circuit implement.

Solution

This is the ‘Sum’ bit of a one bit carry-in adder. A pass transistor implementation is shown below. The transmission gate implementation you designed will have a PMOS in parallel with each NMOS driven by the complement of the signal that drives the NMOS.
b) Now, design a DCVSL gate which implements the same function. Assume $A$, $B$, $C$, and their complements are available as inputs.

**Solution**

One implementation of this circuit is shown on page 50 of Handout #3.

c) Simulate your DCVSL implementation in HSPICE with 30 fF load capacitance on each output. Assume that $W/L = 0.5\mu/0.25\mu$ for all NMOS transistors and $W/L = 2\mu/0.25\mu$ for all PMOS. Does your circuit work? If not, explain why and resize the PMOS devices to fix the problem.

**Solution**

The circuit will not work with this sizing because the PMOS is too large and the NMOS pull-down network will be unable to pull the outputs down to the required value for switching to occur. A more reasonable size for the PMOS is around 0.5 um.

d) Assuming $W/L = 0.5\mu/0.25\mu$ for all nmos transistors and $W/L = WP/0.25\mu$ for the pmos transistors (where WP is the value you chose in part c), produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1. Extract and simulate your circuit to verify functionality.

**Solution**

One possible layout is shown below:
For these problems you should use the parameters for the 0.25 technology (given in the text) unless otherwise specified for a particular problem.

Problem 1: Subthreshold Inverter Operation

In circuit applications where extremely low power consumption is essential and high speed operation is not required, subthreshold logic may provide an ideal solution. This problem will explore how far the supply voltage may be lowered before a CMOS inverter fails. For the entire problem, assume that the both devices are minimum length and that the NMOS device has a width of 0.44 um. Failure is defined as the point where an input swing of 0 to VDD produces an output swing less than 10% to 90% of VDD. For this problem use the 0.18 micron technology file which is located in “/mit/6.374/models/log018_1.l” (Research by Alice Wang)

a) Consider the case where the input to the inverter is 0 V. Will the output voltage remain equal to the supply voltage as the supply voltage is lowered to arbitrarily low values? If not, explain what will happen and why. Would using a wider PMOS device increase or decrease the minimum possible supply voltage? Which process corner (TT, FF, SS, SF, or FS) will be the worst case and why? (Variable process conditions may result in a case where the NMOS and PMOS devices have modified mobilities. TT is the case where both devices are typical, SF has slow NMOS and fast PMOS, etc...)

b) Consider the case where the input to the inverter is VDD. Would using a wider PMOS increase or decrease the minimum supply voltage in this case? Which process corner will be the worst case and why?

c) Now, use HSPICE to simulate the inverter and find the lowest possible supply voltage. Complete one simulation for each input value using the process corners you chose in parts a and b. Use a .DATA statement to vary the width of the PMOS device across the set {0.5u, 1u, 1.5u, 2u, 4u, 8u, 10u, 15u, 30u, 45u, 60u} and sweep VDD from 100mV to 400 mV. Then, using the expressions function in AWaves, plot the ratio of V(out)/VDD. The points where the ratio crosses 0.1 and 0.9 are the failure points. Create a table with three columns containing: PMOS width, minimum supply voltage for the case where the input voltage equals 0, and minimum supply voltage for the case where the input voltage equals VDD.

d) Now use your favorite graphing program (Matlab, Excel, etc....) to create a graphical representation for the functional region of operation. On a single graph, plot both cases (minimum supply voltage, PMOS width) and indicate the region where both conditions are met. What is the lowest possible supply voltage that meets both conditions? What must the PMOS width be to operate at this supply voltage?
Problem 2: CMOS Logic

Consider the following CMOS logic circuits:

![Circuit A](image1.png)  
![Circuit B](image2.png)

Figure 0.1: Two static CMOS gates.

a) Do the two circuits in Figure 0.1 implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

b) Assuming we can ignore all second order effects, do these two circuits have the same output resistances when driven with the same input patterns?

c) Assume the transistors have been sized to give a worst case output resistance of 13 kΩ for the worst-case input pattern. What input patterns \((A, E)\) give the lowest output resistance when the output is low? What is the value of that resistance?

d) What input patterns \((A, E)\) give the lowest output resistance when the output is high? What is the value of that resistance?

e) Neglecting parasitics and assuming a load capacitance of 100 fF, find the best case and worst case \(t_{plh}\) and \(t_{phl}\).

f) Now consider a few second order effects on the propagation delays. Which circuit is optimized for the case when it is known a priori that E will be the last input to arrive and why? How will body effect influence the performance of Circuit A vs. Circuit B?

g) For parts g and h, consider only Circuit B. Each intermediate node has some parasitic capacitance that must be charged and discharged at each transition. Therefore, the propagation delay is a function of both the initial voltage conditions on the internal nodes and the inputs. The initial voltage conditions, however, are determined by the previous inputs. Which set of previous and current inputs will cause the slowest \(t_{plh}\)? Which will cause the slowest \(t_{phl}\)?

h) Let all devices be minimum length and set the widths according to the relative scale in the diagram with \(1=0.375\ um\), specify your source and drain areas and perimters, and include an additional 10 fF load.
Use Nanosim to verify functionality by creating an input file which tests the following set of inputs \([\text{ABCDE}]=[00000, 00001, 11110, 11100, 11111]\). Verify that your simulated output values match the expected logic function. Submit your Nanosim output file.

**Problem 3: Pseudo-NMOS Logic**

Consider the circuit of Figure 0.2.

a) What is the output voltage if only one input is high? If all four inputs are high?

b) What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

c) Compare your analytically obtained results to a SPICE simulation.

![Figure 0.2 Pseudo-NMOS gate.](image)

**Problem 4: Pass Transistor Logic and Level Restoration**

Consider the circuit of Figure 0.3. Assume the inverter switches ideally at \(V_{DD}/2\), neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

![Figure 0.3 Level restoring circuit.](image)

a) What is the logic function performed by this circuit?

b) Explain why this circuit has non-zero static dissipation.
c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

d) Implement the same circuit using transmission gates.

e) Replace the pass-transistor network in Figure 0.3 with a pass transistor network that computes the following function: \( x = ABC \) at the node \( x \). Assume you have the true and complementary versions of the three inputs \( A, B \) and \( C \).

**Problem 5: Device Modeling - DIBL**

The standard equation for modeling subthreshold leakage current given in the notes is

\[
I_d = I_o \cdot e^{\frac{V_{GS} - V_T}{nV_{th}} \cdot \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)}.
\]

This equation does not account for higher order effects like DIBL. The following BSIM equation adds the DIBL effect to the model:

\[
I_d = I_o \cdot e^{\frac{V_{GS} - V_T - (\gamma \cdot V_{SB}) + \eta \cdot V_{DS}}{nV_{th}} \cdot \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)}.
\]

Using this new equation, we will produce a model for the subthreshold leakage in the 0.25 \( \mu \)m process used in 6.374.

a) Using HSPICE, plot \( I_d \) vs \( V_{GS} \) for a single NMOS device with \( V_D = V_{DD} = 2.5V \) and \( W/L = 0.5\mu m/0.25\mu m \). We are only interested in the subthreshold region, so sweep \( V_{GS} \) over the appropriate range.

Using HSPICE, plot \( I_d \) vs \( V_{DS} \) for \( V_{GS} = 0V \) over the full range of \( V_{DS} \). Plot the current on a log scale for both plots.

You will need to extract the points along these curves to use in your favorite analysis program (ie Matlab) for the rest of this problem. The following statement in HSPICE prints a table of the sweeping value and the current through a MOSFET to the HSPICE output stream: .print dc i(Mn1)

b) Using the data from the \( I_d \) vs \( V_{GS} \) plot, extract a value for \( S \), the subthreshold slope, in mV/decade. Plot \( S \) as it varies with \( V_{GS} \). Over which range of \( V_{GS} \) is \( S \) likely to be the most accurate for modeling? Plot “instantaneous \( n \)” as it varies with \( S \). Over which range is it likely to be accurate for modeling?

c) Now we will construct a model for the subthreshold behavior of the FET using the BSIM equation. This model should accurately represent the behavior of the FET that you saw in part a). The BSIM equation still is a reasonably low order model, so do not expect your final result to match the plots precisely - just try for a ballpark match. To develop the model, you need to select three parameters: \( n, I_o \), and \( \eta \). The value for \( n \) should be somewhere in the range that you plotted in b). Select \( I_o \) so that the drain current supplied by the model matches the simulated value at \( V_{GS} = V_{T0} \).

**Hints:** Pick an initial value for \( \eta \) and use it with your estimates for \( n \) and \( I_o \) in the model equation for varying \( V_{DS} \). \( \eta \) controls the slope of the curve versus \( V_{DS} \). Once the slopes are roughly equivalent, use your estimate of \( \eta \) to find the current while sweeping \( V_{GS} \). Select values of \( n \) and \( I_o \) that give a good fit. Now use those values in the other case to refine your choice of \( \eta \). Iterate this process a few times until you are satisfied with the models. It is helpful to convince yourself (by experimentation or from the equation) of the effects of the different param-
eters on the current. Remember, there is a range of “right” answers to this part of the problem. Also, be glad you don’t do this for a living :)

Turn in a plot of $I_o$ vs $V_{GS}$ with the real data and the model data on the same plot. Do the same for $I_o$ vs $V_{DS}$. What were your values for $I_o$, $n$, and $\eta$? Comment briefly on what you consider to be a “good” fit using this model for this process (ie - is it more important to get the slope right or the actual values? is it better to overestimate or underestimate the current? etc). Why is your model a good choice?

**Problem 6: DCVSL Gate Design**

a) Implement the function $S = ABC + \overline{A}BC + \overline{A}BC + \overline{A}BC$ using transmission gate logic. What function does this circuit implement?

b) Now, design a DCVSL gate which implements the same function. Assume $A$, $B$, $C$, and their complements are available as inputs.

c) Simulate your DCVSL implementation in HSPICE with 30 fF load capacitance on each output. Assume that $W/L = 0.5\mu/0.25\mu$ for all PMOS transistors and $W/L = 2\mu/0.25\mu$ for all PMOS. Does your circuit work? If not, explain why and resize the PMOS devices to fix the problem.

d) Assuming $W/L = 0.5\mu/0.25\mu$ for all nmos transistors and $W/L = WP/0.25\mu$ for the pmos transistors (where $WP$ is the value you chose in part c), produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1. Extract and simulate your circuit to verify functionality.
Problem Set #2: Updates and Frequently Asked Questions

Notes and Hints:

Problem 6:

- *** The expression for $S$ should be read as $S=ABC+(A\cdot \overline{B}\cdot \overline{C})+(\overline{A}\cdot \overline{B}\cdot C)+$ $(\overline{A}\cdot B\cdot \overline{C})$. If you interpreted it as $A\cdot \overline{(B\cdot C)}$ etc and have already completed the layout we'll accept that, but please complete the other parts of the problem for the correct interpretation of $S$.
- This should read just "transmission gate", not "NMOS transmission gate" You may assume inputs and their complements are available as inputs.
- For part c, the sizing should be $W/L=0.5/0.25\mu m$ for all NMOS and $W/L=2\mu m/0.25\mu m$ for all PMOS.
Problem 1: Dynamic Logic I

Consider the conventional N-P CMOS circuit below in which all precharge and evaluate devices are clocked using a common clock $\phi$ and its complement. For this entire problem, assume that the pulldown/pullup network is simply a single NMOS/PMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all $T/2$. Assume that the transitions are ideal (zero rise/fall times).

a) Do any problems occur when the input makes a $0 \rightarrow 1$ transition? What about a $1 \rightarrow 0$ transition? If so, describe what happens and insert one inverter somewhere in the circuit to fix the problem.

b) For your corrected circuit, complete the timing diagram for signals $Out_1$, $Out_2$, $Out_3$, and $Out_4$, when the $IN$ signal goes high before the rising edge of the clock $\phi$. Assume that the clock period is 10 $T$ time units.
b) Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock $\phi$ is initially in the precharge state ($\phi = 0$ with all nodes settled to the correct precharge states), and the block enters the evaluate period ($\phi = 1$). Is there a problem during the evaluate period, or is there a benefit? Explain.

c) Assume that the clock $\phi$ is initially in the evaluate state ($\phi = 1$), and the block enters the precharge state ($\phi = 0$). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

**Problem 2: Leakage Power**

Consider the circuit shown below:

a) What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5$\mu$m/0.25$\mu$m.

b) Let the drain current for each device (NMOS and PMOS) be 1mA for NMOS at $V_{GS} = V_{Tn0}$ and PMOS at $V_{GS} = V_{Tp0}$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL.

c) Suppose the circuit is active for a fraction of time $d$ and idle for $(1-d)$. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr(A=1) = 0.5$, $Pr(B=1) = 0.5$, $Pr(C=1) = 0.5$) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle $d$ for which the active power is equal to the leakage power?

**Problem 3: Multi Threshold CMOS**

Multi Threshold CMOS is a circuit technique that utilizes multiple threshold devices to provide both low leakage and high performance operation. The following problem explores some of the issues involved in MTCMOS circuits, although a more realistic circuit would be more complicated (like an adder or multiplier) instead of the single inverter shown below. For hand calculations, ignore body effect, lambda, and parasitic capacitances.

In the sleep mode, M3 is turned off, and this high Vt device limits the subthreshold leakage current. On the other hand, when the circuit is active, M3 is turned on hard for fast switching operation. For the rest of the problem, assume that M3 is turned on. (i.e. $V_{SleepL} = V_{DD}$)
VDD = 2.5V

\[ W_p/L_p = 1.25 \mu m/0.25 \mu m \]
\[ V_{tnl} = -0.2V \]

\[ W_n/L_n = 0.625 \mu m/0.25 \mu m \]
\[ V_{tnl} = 0.2V \]

\[ M_3 \]
\[ W_{nsleep}/L_{nsleep} = 0.625 \mu m/0.25 \mu m \]
\[ V_{tnh} = 0.43V \]

\[ C_1 = 40fF \]

Parts a) through f) do not require HSPICE.

a) What is the desired region of operation for M3 during the active mode?

b) Calculate the effective resistance looking into the drain of transistor M3.

c) Now assume the effective resistance of M3 is 0. What is the peak current (saturation current) that discharges \( C_1 \) during an output high to low transition?

d) What is the peak current taking into account the finite sleep resistance (computed in part b)

e) As \( W_{nsleep} \) increases, qualitatively how does \( t_{PHL} \) vary? How does \( t_{PLH} \) vary?

f) If there is a large parasitic capacitance at node \( V_x \), what is the effect on switching performance?

For HSPICE simulations use the models’ file “logiclvt.l”. Include two .lib statements, one with TT and one with TT_LVT and use nchltv, phlvt, and nch as the three device types in your netlist.

g) Using HSPICE, simulate the circuit for varying \( W_{nsleep} \) values of (0.625u, 1.5u, 3u, 5u, 7u, 9u, 11u). Turn in plots showing output voltage as a function of time and \( V_x \) as a function of time (with the varying \( W_{nsleep} \) curves superimposed on the same graph). Note if done correctly, HSPICE need only be run once. For the input specification, use the piecewise linear option: “Vin node1 node2 pl 0v 0n, 0v 2.5n, 2.5v 2.6n, 2.5v 7.5n, 0v 7.6n”

h) Plot \( t_{PHL} \) and \( t_{PLH} \) for each of these choices of \( W_{nsleep} \)

Problem 4: Low-Swing Bus Drivers

Consider the two possible bus driver circuits shown below:
**Problem 5: Dynamic Logic II**

The figure below shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: \( AD = AS = W \times 0.625 \mu m \) and \( PD = PS = W + 1.25 \mu m \). Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

---

**Use 0.25 um technology: VDD=2.5 V**

**Circuit A**

- **In1**
  - \( C = 1 \) pF

- **In2**
  - \( C = 1 \) pF

**Circuit B**

- **In1**
  - \( C = 1 \) pF

- **In2**
  - \( Cs = 10 \) pF
  - \( C = 1 \) pF

---

a) First consider circuit A. Assume an ideal inputs with zero rise time are available. Assuming \( Wp/Wn = 3 \), find the minimum sized inverters such that \( tp \) will be less than 10% of the period for switching frequencies of 10 MHz, 100 MHz, and 1 GHz. (To make this easy, you can specify \( wn = '0.375u*scale' \) and \( wp = '1.125u*scale' \), specify the areas and perimeters similarly, and just vary the parameter ‘scale’.) What is the average total power consumed by inverters of each of these sizes when the input is low? What is the leakage power consumed by inverters of each of these sizes when the input is low? What is the average total power consumed by the 2-bit bus if the inputs are tied together and switch at a frequency of 100 MHz? (For this very last question, just give a hand calculation based on switching power only and neglecting parasitics.)


c) Now simulate Circuit B with the inputs tied together and switching at 100 MHz. Size the NMOS and PMOS as above and with \( scale = 10 \). Be sure to initialize \( Cs \) to VDD/2 using a .ic statement. In a real circuit you would probably need to use progressively scaled buffers, but for this case you may assume that you have IN1, IN2 and their complements available at the gate inputs with zero rise/fall times. (This means you DO NOT need to implement the two inverters at the input.) How much power do we actually save by using this low-swing driver? Submit your output waveform.

d) What problem might occur in Circuit B if the two inputs had different activity factors?
a) What Boolean functions are implemented at outputs \( F \) and \( G \)? If \( A \) and \( B \) are interpreted as two-bit binary words, \( A = A_1A_0 \) and \( B = B_1B_0 \), then what interpretation can be applied to output \( G \)?

b) Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case.

c) In part c you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock \( \phi \) and its source connected to \( V_{DD} \)) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

d) For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit. Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

e) Using SPICE on the new circuit and applying the sequence of inputs found in part (d), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach ~90% of their final values before evaluation begins. Also, recall that the inputs (\( A, B \) and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

**Problem 6: Dynamic Power**

For parts a and b of this problem, assume independent, identically-distributed uniform white noise inputs.

a) What logical function is implemented by the Circuit A? Does this schematic contain reconvergent fan-out? Explain your answer. Find the exact signal \( P_1 \) and transition \( P_0 \rightarrow 1 \) formulas for nodes \( X, Y, \) and \( Z \) for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation. Assume an np-CMOS implementation with an n-tree first stage.

b) Compute the switching power consumed by Circuit A, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where \( C = 0.3 \ \text{pF} \). Also, assume that \( VDD = 2.5 \ \text{V} \) and that input events occur at a frequency of 100 MHz. Perform this calculation for a static, fully-
complementary CMOS implementation and a dynamic CMOS implementation. Assume np-CMOS again for the dynamic implementation, but find the power for both orders of trees.

![Circuit A](image)

c) Now consider the implementation of a 3-input OR gate shown in Circuit B. Assume that you have 3 inputs A, B, and C and where \(P(A=1)=0.5\), \(P(B=1)=0.2\), \(P(C=1)=0.1\). For a static CMOS implementation of this circuit and neglecting any glitches that may occur, what is the best order to place these inputs in order to minimize power consumption? What is the activity factor at the internal node (INT) in this case? What is the worst order and the activity factor of the internal node in this case?

![Circuit B](image)

Problem 7: Dynamic Logic III

Consider the circuit shown below:

a) Give the logic function of \(x\) and \(y\) in terms of \(A\), \(B\), and \(C\). Sketch the waveforms at \(x\) and \(y\) for the given inputs. Do \(x\) and \(y\) evaluate to the values you expected from their logic functions? Explain.

b) Redesign the gates using np-CMOS to eliminate any race conditions. Sketch the waveforms at \(x\) and \(y\) for your new circuit.
For these problems you can use the process parameters for the 0.25 technology- see the Process Parameters file in the assignments section.

Problem 1: Dynamic Logic I

Consider the conventional N-P CMOS circuit below in which all precharge and evaluate devices are clocked using a common clock $\phi$ and its complement. For this entire problem, assume that the pulldown/pullup network is simply a single NMOS/PMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all $T/2$. Assume that the transitions are ideal (zero rise/fall times).

![Dynamic Logic Circuit Diagram]

a) Do any problems occur when the input makes a 0->1 transition? What about a 1->0 transition? If so, describe what happens and insert one inverter somewhere in the circuit to fix the problem.

Solution

There is no problem if the input makes a 1->0 transition, as long as the input is stable when the evaluate phase begins. However, if the input makes a 0->1 transition, $Out1$ will initially be precharged to 1 and then go to 0 at some time after the evaluate phase begins. In our case this time is $T/2$. This could allow the next
PDN to pull Out2 low before Out1 goes low and cause an error in Out2. Insert the inverter before the PDN generating Out2 to solve the problem.

b) For your corrected circuit, complete the timing diagram for signals Out1, Out2, Out3 and Out4, when the IN signal goes high before the rising edge of the clock φ. Assume that the clock period is 10 T time units

Solution

![Timing Diagram]

b) Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock φ is initially in the precharge state (φ=0 with all nodes settled to the correct precharge states), and the block enters the evaluate period (φ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

Solution

There is no problem during the evaluate stage. The precharged nodes remain charged until a signal propagates through the logic, activating the pull-down network and discharging the node. In fact, this topology improves the circuit’s robustness in terms of charge sharing affecting the output for any generic pull-down network, and reduces the body effect in the pull-down network.

c) Assume that the clock φ is initially in the evaluate state (φ=1), and the block enters the precharge state (φ = 0). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

Solution

There is a problem during the precharge stage. If all precharged nodes are discharged during the evaluate stage, when the precharge FETs simultaneously turn on, the pull-down networks will initially remain on, creating a short circuit. This continues in each gate until the previous gate charges, disabling its pull-down network.

Problem 2: Leakage Power

Consider the circuit shown below:

a) What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5µm/0.25µm.

Solution

\((AB) + C\)
b) Let the drain current for each device (NMOS and PMOS) be 1µA for NMOS at $V_{GS} = V_{Th0}$ and PMOS at $V_{GS} = V_{Tpo}$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL.

**Solution**

When the output is high, the worst-case leakage occurs when two transistors leak in parallel: ABC = 100 or 010. When the output is low, the worst-case leakage also occurs when two transistors leak in parallel: ABC = 110.

c) Suppose the circuit is active for a fraction of time $d$ and idle for $(1-d)$. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($P_r(A=1) = 0.5$, $P_r(B=1) = 0.5$, $P_r(C=1) = 0.5$) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle $d$ for which the active power is equal to the leakage power?

**Solution**

Choose the case where ABC=100.

$$d*P_{active} = (1-d) P_{leakage} \quad P_{active} = \alpha_{0->1}*f_C*V_{DD}^2 = (3/8 * 5/8)*(100*10^6)*(50*10^{-15})*(2.5^2) = 7.3 \mu W.$$  

$$P_{leakage} (ABC = 100) = V_{DD}^2*2*I_{leakM1} = 5*10^{-6} = 251pW.$$  

Plugging the power numbers into the activity equation and solving for $d$ gives $d = 3.4*10^{-5}$.

---

**Problem 3: Multi Threshold CMOS**

Multi Threshold CMOS is a circuit technique that utilizes multiple threshold devices to provide both low leakage and high performance operation. The following problem explores some of the issues involved in MTCMOS circuits, although a more realistic circuit would be more complicated (like an adder or multiplier) instead of the single inverter shown in Figure 1. For hand calculations, ignore body effect, lambda, and parasitic capacitances.

In the sleep mode, M3 is turned off, and this high Vt device limits the subthreshold leakage current. On the other hand, when the circuit is active, M3 is turned on hard for fast switching operation. For the rest of the
VDD = 2.5V

Wp/Lp = 1.25µm/0.25µm
Vthp = -0.2V

Wn/Ln = 0.625µm/0.25µm
Vthn = 0.2V

C1 = 40fF

problem, assume that M3 is turned on. (i.e. V_{SleepL} = VDD)

Parts a) through f) do not require HSPICE.

a) What is the desired region of operation for M3 during the active mode?

Solution

(V_{GS} - V_t) > V_{DSAT} > V_{DS}, therefore M3 is in the linear mode (i.e. M3 acts like a linear resistor).

b) Calculate the effective resistance looking into the drain of transistor M3.

Solution

The effective resistance is just the output resistance of M3 from its corresponding small-signal model:

\[ G = \frac{\partial I}{\partial V_{DS}} = \frac{W_n}{L_n} \cdot (V_{GS} - V_t - V_{DS}) = 115 \times 10^{-6} \times 0.625 \times (2.5 - 0.43) = 595 \times 10^{-6} \quad \text{and} \quad R = G^{-1} \]

R = 1680 Ω. Notice that we assumed the V_{DS} term was negligible. That may not be too valid, but it works for providing an approximation of R.

c) Now assume the effective resistance of M3 is 0. What is the peak current (saturation current) that discharges C1 during an output high to low transition?

Solution

The peak discharge current with the effective resistance of M3 set to 0 is simply the initial discharge current through M2 when M2 is velocity saturated

\[ I_{peak} = k_n \cdot \frac{W_n}{L_n} \cdot V_{DSAT} \cdot (V_{GS} - V_t - 0.5V_{DSAT}) = 115 \times 10^{-6} \times 0.625 \times 0.63 \times (2.3 - 0.315) = 360\mu A \]

d) What is the peak current taking into account the finite sleep resistance (computed in part b)
Solution

With a non-zero effective resistance the voltage at Vx becomes a function of the discharge current and we need to take this into account when determining the peak discharge current.

\[ V_x = iR = 1680i \]

\[ i = k_n \left( \frac{W}{L} \cdot V_{DSAT} \cdot (2.5 - V_x - 0.5 \cdot V_{DSAT}) \right) \]

Solving for \( i \) and \( V_x \), \( V_x = 0.41V \), \( i = 244 \mu A \).

e) As \( W_{nsleep} \) increases, qualitatively how does \( t_{PHL} \) vary? How does \( t_{PLH} \) vary?

Solution

\( t_{PHL} \) decreases, because average current gets bigger. \( t_{PLH} \) is unaffected.

f) If there is a large parasitic capacitance at node Vx, what is the effect on switching performance?

Solution

The switching performance improves (i.e., \( t_{PHL} \) decreases) if there is big capacitance at x. This is because the average current gets larger. If there’s a capacitance at node x then the discharge current entering node x sees a first order RC circuit and as a result Vx increases slowly. This results in a larger \( V_{GS,M2} \) which results in a larger peak current (another way to think about this is to consider the large parasitic capacitor at Vx as a local sink for the charge from Out). The larger the value of the capacitor, the more slowly that Vx will charge and hence the smaller \( t_{PHL} \) becomes.

For Hspice simulations use the models’ file “logiclvt.l”. Include two .lib statements, one with TT and one with TT_LVT and use nchlvt, pchlvt, and nch as the three device types in your netlist.

g) Using HSPICE simulate the circuit for varying Wnsleep values of (0.625, 1.5u, 3u, 5u, 7u, 9u, 11u). Turn in plots showing output voltage as a function of time and Vx as a function of time (with the varying Wnsleep curves superimposed on the same graph). Note if done correctly, HSPICE need only be run once. For the input specification, use the piecewise linear option: “Vin node1 node2 pl 0v 0n, 0v 2.5n, 2.5v 2.6n, 2.5v 7.5n, 0v 7.6n”.

Solution

Figure 2 shows the required plot generated by Hspice.
We can see from the above graph that (f) is verified. (i.e., as parasitic capacitance \( W \) gets bigger \( t_{PHL} \) decreases) Notice that our calculation for \( V_x \) overestimated the value. That is because we assumed \( V_x \) was small enough to neglect when solving for \( R \). In reality, that approximation caused us to underestimate the resistance.

h) Plot \( t_{PHL} \) and \( t_{PLH} \) for each of these choices of \( W_{sleep} \).

**Solution**
Problem 4: Low-Swing Bus Drivers

Consider the two possible bus driver circuits shown below:

Use 0.25 um technology: VDD=2.5 V

Circuit A

In1

C=1pF

In2

C=1pF

C=1pF

C=10pF

C=1pF

Circuit B

a) First consider circuit A. Assume an ideal inputs with zero rise time are available. Assuming Wp/Wn=3, find the minimum sized inverters such that tp will be less than 10% of the period for switching frequencies of 10 MHz, 100 MHz, and 1 GHz. (To make this easy, you can specify wn='0.375u*scale' and wp='1.125u*scale', specify the areas and perimeters similarly, and just vary the parameter 'scale'.) What is the leakage power consumed by inverters of each of these sizes when the input is low? What is the average total power consumed by the 2-bit bus if the inputs are tied together and switch at a frequency of 100 MHz? (For this very last question, just give a hand calculation based on switching power only and neglecting parasitics.)
Solution

Using HSPICE and parameterizing the device sizes in terms of the scale factor it is relatively easy to iterate and find a solution. We find that scale must be about 1 for 10 MHz operation, 7 for 100 MHz operation, and 80 for 1 GHz operation. The leakage currents/powers, measured by placing a zero volt test source between VDD and the PMOS device, are 118 pA/295 pW, 18 pA/45 pW, and 8 pA/20 pW for the required scale factors. (These values for scale and resulting current/power are somewhat subjective The average power of the 2-bit bus can be found by the following method. Each time a capacitor charges from 0->VDD, the required charge is \( Q = CV_{DD} \). For each of the two capacitors this will happen 100E6 times per second, so \( I_{tot} = 2 \times 100E6 \times CV_{DD} \). Then multiply this by VDD since \( P = IV \). The result is that the switching power for the bus is 1.25 mW.


Solution

This circuit works by lowering voltage swing and recycling charge to conserve power. The large capacitor at the middle node acts as a virtual ground at VDD/2 which stores and reuses charge and each of the buses has a swing of VDD/2. The power can be calculated by recognizing that when the two buses make a simultaneous 0->1 transition, the only charge drawn from the supply is \( Q = CV \), where \( \Delta V \) is the change in voltage on the upper bus and is equal to \( V_{DD}/2 \). Then \( I = 100E6 \times C \times \Delta V \) and \( P = 100E6 \times C \times \Delta V \times V_{DD}/2 = 50E6 \times C \times V_{DD}^2 \). This is a factor of 4 reduction in power or 75% savings.

c) Now simulate Circuit B with the inputs tied together and switching at 100 MHz. Size the NMOS and PMOS as above and with scale=10. Be sure to initialize Cs to VDD/2 using a .ic statement. In a real circuit you would probably need to use progressively scaled buffers, but for this case you may assume that you have IN1, IN2 and their complements available at the gate inputs with zero rise/fall times. (This means you DO NOT need to implement the two inverters at the input.) How much power do we actually save by using this low-swing driver? Submit your output waveform.

Solution

The output waveform is shown below. The power, found by averaging the current sourced by VDD, is 294 uW for Circuit B. This is approximately 76.5% percent savings from the theoretical power used by the simple dual inverter bus driver which matches well with the calculated result.
d) What problem might occur in Circuit B if the two inputs had different activity factors?

Solution

If the circuits two inputs had different activity factors the virtual ground capacitor would start to move away from VDD/2 until the circuit failed. For this reason, the actual circuit proposed in the paper has additional biasing circuitry to guarantee that the virtual ground node will remain within a predetermined voltage range.

Problem 5: Dynamic Logic II

Figure 5 shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: $AD = AS = W \times 0.625\mu m$ and $PD = PS = W + 1.25\mu m$. Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

a) What Boolean functions are implemented at outputs $F$ and $G$? If $A$ and $B$ are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output $G$?

Solution

$$F = A_0B_0 + \overline{A_0B_0}, \quad G = F(A_1B_1 + \overline{A_1B_1})$$

If $A$ and $B$ are interpreted as two-bit binary words, output $G$ is high if $A = B$: a comparator.
b) Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case.

![Diagram of the circuit showing two gates with labels and voltages.]

**Solution**

Gate 2 has the higher potential for harmful charge sharing because the capacitance that contributes to charge sharing is larger than in gate 1.

The sequence of inputs resulting in the worst-case charge sharing is \( A_0 \neq B_0 \) and \( A_1 = B_1 \) for the first cycle. Then \( A_0 = B_0 \) and \( A_1 \neq B_1 \) for the second cycle such that \( A_1 / A_I \) transistor that is on during the second cycle is the same as in the first cycle. For example, \( A_1 = B_1 = V_{DD} \) in cycle 1 and \( A_I = V_{DD}, B_I = 0 \) V in cycle 2. This will cause the charge at the output of gate 2 to be shared with the total parasitic capacitance at the drains of the \( A_I, A_I, \) and \( B_I \) transistors.

![Waveform diagram showing the voltage vs. time for the circuit.]

**c)** In part b you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock \( \phi \) and its source connected to \( V_{DD} \)) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this...
addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

Solution

The additional precharge transistor should charge the node that is shared by the \( A_1 \) and \( \overline{A}_1 \) transistor drains and the \( F \) transistor source. Assuming the gate delay is dominated by the precharge stage, this will reduce the gate delay by briefly aiding the precharging of gate 2. SPICE output with additional precharge transistor.

d) For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit. Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

Solution

The worst-case delay results from \( A = B \) for two consecutive cycles. This results in the maximum charging and discharging of the internal nodes.

e) Using SPICE on the new circuit and applying the sequence of inputs found in part (d), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach \( \sim 90\% \) of their final values before evaluation begins. Also, recall that the inputs (\( A, B \) and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

Solution

The maximum clock frequency is \( \sim 4.4 \) GHz if you didn’t include parasitic capacitance. If you did, it is around 2 GHz depending on the assumptions you made.

Problem 6: Dynamic Power

For parts a and b of this problem, assume independent, identically-distributed uniform white noise inputs.
a) What logical function is implemented by the Circuit A? Does this schematic contain reconvergent fan-out? Explain your answer. Find the exact signal \( P_1 \) and transition \( P_0 \rightarrow 1 \) formulas for nodes \( X, Y, \) and \( Z \) for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation. Assume an np-CMOS implementation with an n-tree first stage.

**Solution**

This schematic has reconvergent fan-out because both inputs of the or gate depend on the value of \( S \). However, due to the special nature of this particular case, conditional probability is NOT required to complete the solution.

Assuming a fully complementary CMOS implementation:

\( X \) is the output of an AND gate with independent, identically-distributed uniform white noise inputs. As only when both inputs are equal to 1 the output is 1, \( P_1 = 0.25 \). On the other hand \( P_0 \rightarrow 1 = P_0 P_1 = 0.25(1 - 0.25) = 0.1875 \).

\( Y \) is also the output of an AND gate with independent, identically distributed uniform white noise inputs. The analysis is the same as with \( X \).

If we represent the truth table of the schematic we will see that \( P_1 = 0.5 \). Then \( P_0 \rightarrow 1 = P_0 P_1 = 0.5(1 - 0.5) = 0.25 \).

Assuming a dynamic CMOS implementation:

In the same way as before, for \( X \), \( P_1 = 0.25 \). In order to obtain the transition probability, an n-tree dynamic gate will be assumed. In this case: \( P_0 \rightarrow 1 = P_0 = 0.75 \).

The analysis for \( Y \) is equal to the analysis for \( X \).

For \( Z \), using the truth table of the schematic we obtain, again, \( P_1 = 0.5 \). For the transition probability, it will be assumed that a np-CMOS structure is used. Then, \( Z \) is the output of a p-tree dynamic gate. Then: \( P_0 \rightarrow 1 = P_1 = 0.5 \).

b) Compute the switching power consumed by Circuit A, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where \( C = 0.3 \) pF. Also, assume that VDD = 2.5 V and that input events occur at a frequency of 100 MHz. Perform this calculation for a static, fully-
complementary CMOS implementation and a dynamic CMOS implementation. Assume np-CMOS again for the dynamic implementation, but find the power for both orders of trees.

Solution

i) A static, fully-complementary CMOS implementation.

Switching power is:

\[ P_{SW} = \alpha \cdot f \cdot C \cdot V_{DD}^2 = (\alpha_{X0 \rightarrow 1} + \alpha_{Y0 \rightarrow 1} + \alpha_{Z0 \rightarrow 1}) \cdot f \cdot C \cdot V_{DD}^2 \]

We calculated previously the probabilities of a 0->1 transition for each node: \( P_{0 \rightarrow 1} \) for X and Y is 0.1875 and \( P_{0 \rightarrow 1} \) for Z is 0.25.

Thus, \( P_{SW} = (2*0.1875+0.25)*100MHz*0.3pF*2.5^2 = 117.2uW \).

ii) A dynamic CMOS implementation

In part b) for a dynamic np-CMOS gate, we calculated the probabilities: \( P_{0 \rightarrow 1} \) for X and Y is 0.75 and \( P_{0 \rightarrow 1} \) for Z is 0.5. Thus, \( P_{SW} = (2*0.75+0.5)*100MHz*0.3pF*2.5^2 = 375uW \).

When the first stage is implemented with a p-tree, \( P_{0 \rightarrow 1} \) is equal to \( P_1 = 0.25 \). The output stage has \( P_{0 \rightarrow 1} \) equal \( P_0 = 0.5 \). Thus,

\[ P_{SW} = (2*0.25+0.5)*100MHz*0.3pF*2.5^2 = 187.5uW \].

c) Now consider the implementation of a 3-input OR gate shown in Circuit B. Assume that you have 3 inputs A, B, and C and where \( P(A=1) = 0.5 \), \( P(B=1) = 0.2 \), \( P(C=1) = 0.1 \). For a static CMOS implementation of this circuit and neglecting any glitches that may occur, what is the best order to place these inputs in order to minimize power consumption? What is the activity factor at the internal node (INT) in this case? What is the worst order and the activity factor of the internal node in this case?

Circuit B

![Circuit B Diagram]

Solution

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<th>( P(1) ) for INT</th>
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</tbody>
</table>

So, to minimize power consumption we should place B and C at the first stage. The worst case occurs when A and C placed at the input stage. The activity factors for each case are shown in the table above.
Problem 7: Dynamic Logic III

Consider the circuit shown below:

a) Give the logic function of \(x\) and \(y\) in terms of \(A\), \(B\), and \(C\). Sketch the waveforms at \(x\) and \(y\) for the given inputs. Do \(x\) and \(y\) evaluate to the values you expected from their logic functions? Explain.

Solution

\(x = \overline{A}B\) and \(y = AB\overline{C}\)

The circuit does not correctly implement the desired logic function. This stems from the fact that \(x\) is pre-charged high, and thus node \(y\) is discharged as soon as the evaluation phase starts. Although \(x\) is eventually discharged by the first stage, \(y\) cannot be charged high again since it is a dynamic node with no low-impedance path to Vdd (during evaluate). Common solutions to this problem are to place an inverter between the two stages (thus allowing only 0-to-1 transitions on the inputs to each stage during evaluate) as in Domino logic or employ np-CMOS. The latter is presented in (b).

b) Redesign the gates using np-CMOS to eliminate any race conditions. Sketch the waveforms at \(x\) and \(y\) for your new circuit

Solution.
FAQs and Overview of Problem Set 3

Notes and Hints:

Problem 1:

• The statement that "each stage consist of a dynamic inverter followed by a static inverter" is in error. For this particular logic style we do not need static inverters except in the one place you choose.

Problem 2:

• For part (c) you may assume S=100mV/decade. Also for part (c), choose the input vector that you chose in part (b) for the worst case leakage through the pull-up network when the output=0V

Problem 3:
Problem 4:

• Leakage power may be found by simulation.
• For the hand calculation of power, you may assume that the 10 pF node is always equal to VDD/2, despite the fact that in practice it varies by about 100 mV during switching.

Problem 5:
Problem 6:

• You may assume that CL=0 when running your simulations.

Problem 7:
Problem 1: MTCMOS Sleep Device Sizing

This problem examines sizing for MTCMOS sleep devices in a cutting edge technology. The devices in the problem are 0.07 µm FETs modeled by a Predictive BSIM model. We generated the predicted models using Berkeley Predictive Technology Model (http://www-device.eecs.berkeley.edu/~ptm/introduction.html). You may find this site useful for generating models to use in your project.

Please use the following assumptions in this problem:
- Every inverter has a fanout of 4. The gate capacitance of an inverter can be approximated as 0.7fF/FET.
- All LVT inverters have PMOS W/L = 0.22um/0.07um and NMOS W/L = 0.1um/0.07um.
- VDD=1.2V.
- AS=AD=6*λ*W and PS=PD=10*λ + W.
- The minimum grid size is 0.0025um. In other words, the width of your FETs should be N*0.0025um, N=integer.
- To get the model files, type the following four lines in HSPICE deck:
  .include 'nfet007hvt.l'
  .include 'nfet007lvt.l'
  .include 'pfet007hvt.l'
  .include 'pfet007lvt.l'
- To instantiate a FET, use the following names: NMOSht, NMOSlt, PMOSht, PMOSlt.
- When finding leakage, assume VGS=0. Measure leakage for the input that gives the worst-case improvement.
- HINT: Use subcircuits to make your life easier. The documentation on the webpage shows how.
- HINT: To simulate settling leakage currents, add the following lines to your HSPICE deck:
  .options accurate
  .options method=gear

a) For the circuits in Figure 1, use HSPICE to find a size for MNS and another for MPS such that the inverters only see...
10% reduction in propagation delay. Repeat your simulation to find sizes to achieve only 5% degradation in $t_p$. Turn in ONLY the following:
i) Fill out Table 1.
ii) Transient simulation plot showing $I_D$ settle to the sleep value when the inverter enters sleep mode. Use the drain current in the NMOS device in the inverter for your measurements. Show the current settling for all four cases on one plot (PMOS 5%, PMOS 10%, NMOS 5%, NMOS 10%). Use a SEMILOG plot (Y-axis log).

### Table 1: Results from Part (a)

<table>
<thead>
<tr>
<th>Delay Penalty</th>
<th>$M_{NS}$ (um)</th>
<th>$M_{PS}$ (um)</th>
<th>$I_{DBASE}$ (nA)</th>
<th>$I_{DNS}$ (nA)</th>
<th>$I_{DPS}$ (nA)</th>
<th>$I_{DBASE}/I_{DNS}$ (X)</th>
<th>$I_{DBASE}/I_{DPS}$ (X)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 2:** Sizing Sleep Devices for Parallel and Series Inverters

b) Refer to Figure 2. Use HSPICE to size $M_{NSER}$ and $M_{NPAR}$ for both cases to achieve 5% and 10% delay degradation over the appropriate base case. Turn in ONLY the following:
i) Fill out Table 2.

### Table 2: Results from Part (b)

<table>
<thead>
<tr>
<th>Delay Penalty</th>
<th>Parallel $M_{NPAR}$ (um)</th>
<th>Series $M_{NSER}$ (um)</th>
<th>$I_{DBASE}$ (nA)</th>
<th>$I_{DSER}$ (nA)</th>
<th>$I_{DPAR}$ (nA)</th>
<th>$I_{DBASE}/I_{DSER}$ (X)</th>
<th>$I_{DBASE}/I_{DPAR}$ (X)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

c) Refer to Figure 3. Try to minimize standby leakage current. You may use any number of sleep devices with or without sharing. You also may insert a 2-input gate into the dotted box. Use HSPICE to minimize standby leakage current while maintaining no more than a 10% delay penalty. Turn in ONLY the following:
i) A schematic of the circuit including the sleep devices and their sizes.
ii) The total width of the sleep devices.
iii) The total leakage savings in standby mode relative to active mode leakage (in X, for worst-case).
iv) A transient simulation showing the total leakage current settling to its steady-state value when the circuit enters sleep. Use a SEMILOG plot (Y-axis).
Problem 2: Adder Design

You are to design, layout, and simulate an **16-bit ripple carry adder** with the following specifications:

Table 3: Input/Output Signals

<table>
<thead>
<tr>
<th>Input</th>
<th>Description</th>
<th>Output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B[15:0]</td>
<td>15-bit operand</td>
<td>Co</td>
<td>Carry out</td>
</tr>
<tr>
<td>Ci</td>
<td>Carry in</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Your inputs have to go through two minimum length inverters \((W_p/W_n=1.125/0.375)\) before driving the adder inputs in your netlist (do **NOT** layout these inverters). All outputs have a capacitive load of 30fF.

a) Layout the adder in MAGIC using **ANY** static CMOS logic style with rail to rail outputs.
Your goal is to **minimize energy/addition** meeting a specific delay constraint, by lowering $V_{dd}$ and/or by your choice of static circuit style. The worst case critical path delay must be $t_p \leq 4\text{ns}$. Observe good layout techniques that reduce parasitic capacitances and resistances. Turn in **ONLY**:

i) a schematic of your 1-bit adder implementation

ii) the layout of the 1-bit adder and its area

iii) the layout of the full 16-bit adder and its area

After problem set 2 you have become experts in layout, so your layout should be compact and not excessively spread out. This time there will be points off for unnecessary wasted area (money).

You must print a **color** version of your layout.

b) Extract and verify that your adder works. You have to use the input vector file located in: `input.vec`. Use SimWave to view your nanosim waveforms. (see FAQ for details). Does your adder work? (Yes/No).

c) Determine the critical path in the circuit (tell us the input vectors that give the worst case delay), and simulate the extracted circuit in HSPICE with the input pattern displaying the critical path. Turn in a plot showing the worst case propagation delay of your adder.

d) Using the input vector file located in: `input.vec`, report the dissipated power at $V_{dd} = 2.5\text{V}$, when the input frequency is 100Mhz. What is the average energy per addition?

e) Using the input vector file located in: `input.vec`, report the dissipated power at your desired power supply voltage, when the input frequency is 100Mhz. Your design must meet the delay constraint ($t_p \leq 4\text{ns}$), at this operating voltage (see part(c)). What is the average energy per addition?

**Layout Requirements**

All A,B inputs should come in from the top of the cell in metal 1 or 2. All S outputs should come out from the bottom of the cell in metal 1 or 2.

**Useful hints and suggestions:**

- To find out your plot area in MAGIC use macro ‘f’ followed by ‘b’. This selects your cell and ‘boxes’ it. You should get the area of the box in terms of your grid size.
- Remember device sizes in Magic are multiples of lamda.
Problem 1: MTCMOS Sleep Device Sizing

This problem examines sizing for MTCMOS sleep devices in a cutting edge technology. The devices in the problem are 0.07μm FETs modeled by a Predictive BSIM model. We generated the predicted models using Berkeley Predictive Technology Model (http://www-device.eecs.berkeley.edu/~ptm/introduction.html). You may find this site useful for generating models to use in your project.

Please use the following assumptions in this problem:
- Every inverter has a fanout of 4. The gate capacitance of an inverter can be approximated as 0.7fF/FET.
- The inverter has PMOS W/L = 0.22um/0.07um and NMOS W/L = 0.1um/0.07um.
- VDD=1.2V.
- AS=AD=6*λ *W and PS=PD=10*λ + W.
- The minimum grid size is 0.0025um. In other words, the width of your FETs should be N*0.0025u, N=integer.
- To get the model files, type the following four lines:
  .include 'nfet007hvt.l'
  .include 'nfet007lvt.l'
  .include 'pfet007hvt.l'
  .include 'pfet007lvt.l'
- To instantiate a FET, use the following names: NMOShvt, NMOSlvt, PMOShvt, PMOSlvt.
- When finding leakage, assume VGS=0. Measure leakage for the input that gives the worst-case improvement.
- HINT: Use subcircuits to make your life easier. The documentation on the webpage shows how.
- HINT: To simulate settling leakage currents, add the following lines to your spice deck:
  .options accurate
  .options method=gear

a) For the circuits in Figure 1, use HSPICE to find a size for MNS and another for MPS such that the inverters only see 10% reduction in propagation delay. Repeat your simulation to find sizes to achieve only 5% degradation in \( t_p \). Turn
in ONLY the following:
i) Fill out Table 1.
ii) Transient simulation plot showing $I_D$ settle to the sleep value when the inverter enters sleep mode. Use the drain current in the NMOS device in the inverter for your measurements. Show the current settling for all four cases on one plot (PMOS 5%, PMOS 10%, NMOS 5%, NMOS 10%). Use a SEMILOG plot (Y-axis log).

SOLUTION:

<table>
<thead>
<tr>
<th>Delay Penalty</th>
<th>$M_{NS}$ (um)</th>
<th>$M_{PS}$ (um)</th>
<th>$I_{DBASE}$ (nA)</th>
<th>$I_{DNS}$ (nA)</th>
<th>$I_{DPS}$ (nA)</th>
<th>$I_{DBASE}/I_{DNS}$ (X)</th>
<th>$I_{DBASE}/I_{DPS}$ (X)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5%</td>
<td>0.44</td>
<td>1.4375</td>
<td>9.9718 (in=1) 8.2115 (in=0)</td>
<td>1.032 (in=1) 1.389 (in=0)</td>
<td>9.66</td>
<td>5.91</td>
<td></td>
</tr>
<tr>
<td>10%</td>
<td>0.2325</td>
<td>0.725</td>
<td>9.9718 (in=1) 8.2115 (in=0)</td>
<td>0.706 (in=1) 1.043 (in=0)</td>
<td>14.12</td>
<td>7.87</td>
<td></td>
</tr>
</tbody>
</table>

These numbers depend reasonably strongly on the measured propagation delay (which varies with the transient step size). Do not worry if your numbers are different as long as they are in the right vicinity.
b) Refer to Figure 2. Use HSPICE to size $M_{NS}$ for both cases to achieve 5% and 10% delay degradation over the appropriate base case. Turn in ONLY the following:
i) Fill out Table 2.

**SOLUTION:**

**Table 2: Results from Part (b)**

<table>
<thead>
<tr>
<th>Delay Penalty</th>
<th>R_{Series} M_{NS} (um)</th>
<th>Parallel M_{NSER} (um)</th>
<th>$I_{DBASE}$ (nA)</th>
<th>$I_{DSER}$ (nA)</th>
<th>$I_{DPAR}$ (nA)</th>
<th>$I_{DBASE}/I_{DSER}$ (X)</th>
<th>$I_{DBASE}/I_{DPAR}$ (X)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5%</td>
<td>0.97</td>
<td>0.2975</td>
<td>18.1834 (ser,in=0,1)</td>
<td>0.826 (in=0)</td>
<td>22.01</td>
<td>7.52</td>
<td></td>
</tr>
<tr>
<td>10%</td>
<td>0.485</td>
<td>0.165</td>
<td>19.9436 (par,in=1)</td>
<td>0.5774 (in=0)</td>
<td>31.49</td>
<td>11.37</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 2:** Sizing Sleep Devices for Parallel and Series Inverters
c) Refer to Figure 3. You may use any number of sleep devices with or without sharing. You also may insert a 2-input gate into the dotted box. Use HSPICE to minimize standby leakage current while maintaining no more than a 10% delay penalty. Turn in ONLY the following:
i) A schematic of the circuit including the sleep devices and their sizes.
ii) The total width of the sleep devices.
iii) The total leakage savings in standby mode relative to active mode leakage (in X, for worst-case).
iv) A transient simulation showing the total leakage current settling to its steady-state value when the circuit enters sleep. Use a SEMILOG plot (Y-axis).

**Figure 3: Sizing Sleep Device(s) for an Inverter Tree**

**SOLUTION:**

There are many possible solutions to this problem. A few good options are:

- Use 1 PMOS device for the input stage and the output stage. Use one NMOS device for the middle stage. Use a NOR gate at the input with SLEEP as the second input to take advantage of the stack effect. Using this approach, I got 196X leakage savings without much optimizing. The total width was 7.05um so savings were about 28X/um.
- Use 1 PMOS device for the entire thing. Less sleep device area, but leakage dominated by the stage which has no stack effect.
- Same as the top two, but with NMOS and PMOS switched. Advantage: less area. Disadvantage: lower leakage savings.

Since we are supposed to minimize leakage, we DEFINITELY should use the 2-input gate to generate a known input vector during sleep mode. This lets us use the stack effect to our advantage.
**Problem 2: Adder Design**

You are to design, layout, and simulate an **16-bit ripple carry adder** with the following specifications:

<table>
<thead>
<tr>
<th>Input</th>
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<tr>
<td>Ci</td>
<td>Carry in</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 3: Input/Output Signals**

![Diagram of 16-bit ripple carry adder]

Your inputs have to go through two minimum length inverters \( W_p/W_n = 1.125/0.375 \) before driving the adder inputs in your netlist **do NOT** layout these inverters. All outputs have a capacitive load of 30fF.

a) Layout the adder in MAGIC using ANY static CMOS logic style with rail to rail outputs.

Your goal is to **minimize energy/addition** meeting a specific delay constraint, by lowering \( V_{dd} \) and/or by your choice of static circuit style. The worst case critical path delay must be \( t_p \leq 4 ns \). Observe good layout techniques that reduce parasitic capacitances and resistances. Turn in **ONLY**:

i) a schematic of your 1-bit adder implementation

ii) the layout of the 1-bit adder and its area

iii) the layout of the full 16-bit adder and its area

After problem set 2 you have become experts in layout, so your layout should be compact and not excessively spread out. This time there will be points off for unnecessary wasted area (money).

You must print a **color** version of your layout.

**Solution**

There is no wrong or right answer.

We have examined many different adder designs with different trade-offs.
b) Extract and verify that your adder works. You have to use the input vector file located in: input.vec. Use SimWave to view your nanosim waveforms. (see FAQ for details). Does your adder work? (Yes/No).

c) Determine the critical path in the circuit (tell us the input vectors that give the worst case delay), and simulate the extracted circuit in HSPICE with the input pattern displaying the critical path. Turn in a plot showing the worst case propagation delay of your adder.

Solution

The worst case delay for a ripple carry adder, happens when at every one-bit full adder, the carry out bit makes a transition. Assuming equal rise and fall times, a transition that could give the maximum delay for an adder is \(A=0x0000, B=0xffff\) and \(C=0->1\).

d) Using the input vector file located in: input.vec, report the dissipated power at \(V_{dd}=2.5V\), when the input frequency is 100Mhz. What is the average energy per addition?

Solution

The average energy per addition depends on the way that you implemented the adder.

e) Using the input vector file located in: input.vec, report the dissipated power at your desired power supply voltage, when the input frequency is 100Mhz. Your design must meet the delay constraint \((t_p \leq 4ns)\), at this operating voltage (see part(c)). What is the average energy per addition?

Solution

Assuming you met the timing constraint and there was a delay margin that you could exploit, you could lower the supply voltage to reduce the power consumption of your circuit.

Layout Requirements

All A,B inputs should come in from the top of the cell in metal 1 or 2. All S outputs should come out from the bottom of the cell in metal 1 or 2.

Useful hints and suggestions:

• To find out your plot area in MAGIC use macro ‘f’ followed by ‘b’. This selects your cell and ‘boxes’ it. You should get the area of the box in terms of your grid size.
• Remember device sizes in Magic are multiples of lamda.
FAQs and Overview of Problem Set 4

Notes and Hints:

Problem 1:

- Q: What is the grid?
  A: Many modern technologies allow you to layout devices with a finer granularity than lambda. The grid value tells you what the granularity is. As the directions state, the dimensions of your devices should be integer multiples of THE GRID SIZE (Note: The FAQ had a typo for a while - it said lambda. The pset is correct, and this note has been corrected). DO NOT turn in a width that looks like W=1.3532334564355!!!

- Q: Why does the DUT FET only have 3*0.7fF at the input?
  A: READ THE DIRECTIONS! Every FET has a fanout of 4. The inverter driving the DUT drives 3*0.7fF (modeling 3 inverters) plus the DUT (the fourth inverter).

- Q: I'm using a subcircuit in hspice to model the inverter. How can I measure the drain current, Id, on the NMOS device inside the inverter?
  A: You can access nodes inside a subcircuit by using the following notation:
  `.print tran i(xsubcircuitname.mfetname)
  You can access nodes inside nested subcircuits by using more levels with the '.'

- Q: Is the grid size lambda? Is lambda = 0.0025um?
  A: NO! Lambda = 0.035um because the minimum length is 0.07um.

- Q: What does "Measure leakage for the input that gives the worst-case improvement" mean?
  A: Different inputs to the circuits of interest will produce different leakage currents. You should make your measurements using the input that gives the worst-case improvement. You should be able to predict which input this will be - if not, come to office hours or try them all to see.

- Q: My leakage currents settle slowly! When do I measure the leakage?
  A: Measure leakage current once it has settled. You need to set up your simulation to last long enough to see this occur (*many* microsecs). If it is taking forever to run, increase the step size in your .tran statement.

- Q: What t_p do we use? (tpHL+tpLH)/2 or just the affected transition?
  A: The problem says to use t_p which we have defined in class as (tpHL+tpLH)/2.

- Q: In part (c), can we assume a given input?
  A: No. Then you cannot assume anything about the input 'IN'. You may add an
optional 2-input gate, however, and you can connect its second input (IN2) to whatever you wish.

- Q: In table two, should there be separate cases of I_Base for series and parallel?  
  A: Yes. There should be two cases.

Problem 2:

- The input vector file has 33 columns

  The signals in the columns are:  
  A[15:0],B[15:0],Cin

- To run SimWave type the following:  
  athena\setup synopsys  
  synopsys\wd

  This will bring up the waveform viewer.

  To view your outputs, just load the database of your design. The format that you should use is EPIC and you just need to choose the .out file.

- In order to get the wiring capacitances in your Hspice netlist, when extracting from Magic you should use the following command at the Athena prompt.

  ext2spice -o file_name.sp file_name.ext -c 0

- The SUM outputs and the last COUT output should have an additional load of 30fF.  
  Add it manually in your spice deck.

- If you don't have access to a color printer, you can print your design the athena color printer located in the Copy Tech, at the student center

- The power can be found by adding 'report_block_powr total *' as an additional line in your cfg file.
Problem 1: Transmission Gate Register Design

a) What type of register is this? Briefly explain how it works.

b) Your problem is to size the inverters and transmission gates. Assume a supply voltage of 2.5V and fully static inverters. Simulate the circuit in HSPICE with the input waveforms shown in the figure. Assume negligible rise and fall times for the CLK and \( \overline{CLK} \) signals and no skew between them. To begin with assume all NMOS devices to be minimum sized and all PMOS devices to be 3 times the NMOS devices. Assume Q is 0V initially.

Does your circuit work? (There goes my raise!). Turn in plots showing input waveforms along with D and Q signals.

Resize the transistors so that the circuit is functional. Point out the changes you have made and explain clearly. Turn in the same plots as in (b) but simulated with modified sizes.
**Hint:** Do not HSPICE the circuit to death. It would be better if you used .SUBCKT macros and tweaked only those sizes that you think will matter. Think before you simulate!

**Problem 2: Edge Triggered Register**

Consider the following edge-triggered register. Assume that the clock inputs $CLK$ and $\overline{CLK}$ have a 0V to $V_{DD}$ swing. Also assume (for parts a-c) that there is no skew between $CLK$ and $\overline{CLK}$ (i.e., the inverter delay to derive $\overline{CLK}$ from $CLK$ is zero). Assume that the rise/fall times on all signals are zero.

a) What type of register is this? (Positive Edge-Triggered Register or Negative Edge-Triggered Register). Explain.

b) Assume that the propagation delay of each clocked inverter (e.g., $M_1$-$M_4$) is $T_{CK,INV}$ and the delay of inverters $I_1$ and $I_2$ is $T_{INV}$. Derive the expression for the set-up time ($t_{su}$), the propagation delay ($t_{c-q}$) and the hold time ($t_h$) in terms of the above parameters. Explain your results.

c) What is the function of transistors $M_5$-$M_8$ and $M_{13}$-$M_{16}$? Is this circuit Ratioed?

d) Consider the following variation of the circuit in the figure below. If there is a clock overlap, is there a potential problem? If so explain the problem and describe the condition when it happens.
Problem 3: True Single Phase Flip-Flop.

Consider the True Single Phase Flip-Flop shown here:

Simulate the circuit in HSPICE. The sizes of the devices are given in terms of lambda. Make sure you initialize node B and that you use stimuli given below.

```
.ic nB=pvdd
*nb is the node noted B on the schematic
Vclk clk 0 pulse (0 pvdd 10n 0.5n 0.5n 10n 20n)
Vd d 0 pwl(0n 0v 25n 0v 25.5n pvdd 45n pvdd 45.5n 0)
```

Do you see the glitching at the output? Explain what happens. Change the sizes of 2 transistors and fix the glitch.
ing. Turn in a table with the new sizes and a spice plot showing the new glitch-free flip-flop output. For the corrected flip-flop, measure the setup time using HSPICE and report it in the table as well. As a reminder: $AS=AD= W \text{ (in } \mu \text{m)} \times 0.625 \text{ } \mu \text{m}$, $PS=PD= W \text{ (in } \mu \text{m)} + 1.5 \mu \text{m}$

Problem 4: Sequential Circuit

Consider the following sequential circuit. Assume that there is no delay between $D$ and $\overline{D}$ (i.e., the inverter delay to obtain $\overline{D}$ from $D$ is 0). Assume that the output is statically held using circuits not shown here (i.e., ignore leakage effects for this problem). Assume that the rise/fall times on all signals are zero.

a) Complete the following timing diagram for $X$ and $Q$.

Assume that the inverter delay is much smaller than the clock period and that appropriate set-up/hold times are met. Assume that each gate ($I_1$, $I_2$, $I_3$, NOR, $M_1$-$M_4$ and $M_7$-$M_{10}$) takes 1 time unit for a low to high or high to low transition. Also assume that it takes 1 time unit to charge node $X$ through $M_5$ or $M_6$. Both the propagation and contamination (i.e., minimum) delay are equal to 1.

b) What is the set-up time for this circuit if glitches on the output $Q$ are acceptable? Explain.
Problem 5: DEC StrongARM Low Power Edge-Triggered Flip-Flop

The flip-flop shown in the above figure is used in the StrongARM microprocessor developed by Digital Equipment Corporation for the Portable Electronic Device (PED) market. Note that it is fully differential. The following questions will help you understand the operation of this flip-flop. No calculations are necessary for this problem.

a) When clock is low is the flop holding or is it transparent? Why? (2 sentences)

b) What is the purpose of the shorting transistor connecting nodes L3, L4? (2 sentences)

c) What is the main advantage of this flip-flop from a low power perspective? (1 sentence)

d) What determines the setup time for this flip-flop? Draw a timing diagram showing the timing relationship between the data and the clock. (1 sentence)

e) From a system perspective, where should this flip-flop be used (i.e., in datapaths for pipelining, as receivers at the end of long buses, as state bits for FSMs, etc.)? Why? (1 sentence)

Problem 6: Submicron Interconnect Effects.

Consider the following interconnect circuit. $C_L$ is the lumped capacitance of each line to ground and $C_I$ is the inter-wire capacitance. The driver (inverter) is modeled using resistors and an ideal switch. The Switch is ideal and is connected either to the top resistor or the bottom resistor. $R_I$ is the effective resistance of the interconnect. For this problem, let $\lambda = \frac{1}{C_L}$. 
(a) Assume that the initial voltage on line $i$ (where $i = 0$ or 1) is $V_i^{OLD}$ and the final value after all the transients have settled is $V_i^{NEW}$. Derive an expression for the energy drawn from $V_{DD}$ through driver 0 for an arbitrary transition of the two bit bus.

b) Assume that $\lambda = 0$ for this part. The total energy (i.e., including both drivers) drawn from the power supply for a sequence can be written as $\eta \cdot C_L \cdot V_{DD}^2$. Estimate the value of $\eta$ for the following two sequences.

**Sequence A:** 00 → 01 → 11 → 10

**Sequence B:** 00 → 11 → 00 → 11

c) Assume that $\lambda = 3$ for this part. The total energy (i.e., including both drivers) drawn from the power supply for a sequence can be written as $\eta \cdot C_L \cdot V_{DD}^2$. Estimate the value of $\eta$ for the following two sequences.

**Sequence A:** 00 → 01 → 11 → 10

**Sequence B:** 00 → 11 → 00 → 11

d) For the transition of the bus from 01 to 10, compute the total energy dissipated in the resistors.

**Problem 7: Data-Dependent Logic Swing Internal Bus Architecture (DDL Bus)**

Consider the DDL bus architecture for an N bit bus. (Refer to the figures in the lecture notes.)

a) Assuming M bits switched to 0, by what factor do we save power compared to the conventional full swing bus? (remember that there are always 2 bits switching to 0 to provide the “0” and “1” references)

b) What is the range of “0” ref? Why are there two “0” refs?

c) What is the reason for having M2 and M3? Wouldn’t it be enough just to have M1 and M4 charge up the nodes A and B to turn the inverter off during precharge?

The following figure shows the receiver for the DDL bus architecture. (Dual Reference Sense Amplifying

---

Dual reference sense amplifying receiver.
Problem 1: Transmission Gate Register Design

Having mastered the art of register and latch design you are faced with the following problem. Your manager asks you to design a “Reduced Clock Load Transmission Gate Register”. You look up your 6.374 Bible, and Bingo! You have it right there in Handout #7, Slide 24. Good thing you took the class, at least you have the schematic to begin with :) 

![Schematic of Transmission Gate Register](image)

a) What type of register is this? Briefly explain how it works.

Solution

This is a positive edge triggered register. When CLK=0, the first stage (master) is transparent and the second stage (slave) is in the hold mode. When CLK=1 the situation is reversed. Therefore, data is sampled on the positive edge of the clock.

b) Your problem is to size the inverters and transmission gates. Assume a supply voltage of 2.5V and fully static inverters. Simulate the circuit in HSPICE with the input waveforms shown in the figure. Assume negligible rise and fall times for the CLK and CLKB signals and no skew between them. To begin with assume all NMOS devices to be minimum sized and all PMOS devices to be 3 times the NMOS devices. Assume Q is 0V initially. Does your circuit work? (There goes my raise!). Turn in plots showing input waveforms along
with D and Q signals.

**Solution**

The circuit does NOT work with identically sized subckt elements (i.e. where all PMOS devices are 3x the minimum sized NMOS devices within each inverter/transmission gate). The reason why the circuit does not work as it should is because when X1 tries to write a value to node 1 which is different from its initial value, there will be a fight between X3 and X1. To make X1 override we have to make the PDN and PUN of X3 sufficiently weak such that node 1 can be brought up/down to the switching threshold of X2. A similar consideration holds for the case when X2 tries to write a value to node 3 which is different from its initial value. Once again we have to make X5 “weaker” compared to X2.

![Original Device Sizing](image1.png)

### c) Resize the transistors so that the circuit is functional.

*Point out the changes you have made and explain clearly. Turn in the same plots as in (b) but simulated with modified sizes.*

**Hint:** Do not HSPICE the circuit to death. It would be better if you used .SUBCKT macros and tweaked only those sizes that you think will matter. Think before you simulate!

**Solution**

The original and modified sizes are as follows. Instead of considering all transistors, we consider the relative sizes of the transmission gates and inverters. Each of these elements have their PMOS device 3 times the size of
the NMOS device. (Minimum sized element => PMOS : $9\lambda/2\lambda$ and NMOS : $3\lambda/2\lambda$.)

<table>
<thead>
<tr>
<th></th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>X4</th>
<th>X5</th>
<th>TX1</th>
<th>TX2</th>
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<tr>
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<tr>
<td>Modified size (relative)</td>
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<td>1</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

**Problem 2: Edge Triggered Register**

Consider the following edge-triggered register. Assume that the clock inputs $CLK$ and $\overline{CLK}$ have a $0V$ to $V_{DD}$ swing. Also assume (for parts a-c) that there is no skew between $CLK$ and $\overline{CLK}$ (i.e., the inverter delay to derive $\overline{CLK}$ from $CLK$ is zero). Assume that the rise/fall times on all signals are zero.

a) What type of register is this? (Positive Edge-Triggered Register or Negative Edge-Triggered Register). Explain.

**Solution**

Negative Edge-Triggered. Master is transparent and slave is holding when $CLK=1$. Slave is transparent and master is holding when $CLK=0$. 
b) Assume that the propagation delay of each clocked inverter (e.g., $M_1$-$M_4$) is $T_{CK,INV}$ and the delay of inverters $I_1$ and $I_2$ is $T_{INV}$. Derive the expression for the set-up time ($t_{su}$), the propagation delay ($t_{c-q}$) and the hold time ($t_H$) in terms of the above parameters. Explain your results.

**Solution**

**Setup**: Data must go through 1st clocked inverter and $I_1$ so $t_{su} = T_{ck,inv} + T_{inv}$.

**Propagation delay**: $Q$ becomes valid when the data passes through the second clocked inverter so $t_{c-q} = T_{ck,inv}$.

**Hold time**: When CLK goes 1->0, the first clocked inverter is already off, so $t_H = 0$.

c) What is the function of transistors $M_5$-$M_8$ and $M_{13}$-$M_{16}$? Is this circuit Ratioed?

**Solution**

These FETs implement two clocked inverters. Each clocked inverter is on when its respective stage is holding, so they complete a back-to-back inverter pair that makes the circuit static. The circuit is not ratioed because the inverters turn off during the sample operation, so there is never a fight.

d) Consider the following variation of the circuit in the figure below. If there is a clock overlap, is there a potential problem? If so explain the problem and describe the condition when it happens.

**Solution**

In the 1-1 overlap, $D$ can race through and change $Q$. This is a problem because the register is supposed to hold. In the 0-0 overlap, $D$ can race through and change $Q$, but we can fix this with a hold-time constraint.
Problem 3: True Single Phase Flip-Flop.

Consider the True Single Phase Flip-Flop shown here:

Simulate the circuit in HSPICE. The sizes of the devices are given in terms of lamda. Make sure you initialize node B and that you use stimuli given below.

.ic nB=pvdd
*nb is the node noted B on the schematic

Vclk clk 0 pulse (0 pvdd 10n 0.5n 0.5n 10n 20n)
Vd d 0 pwl(0n 0v 25n 0v 25.5n pvdd 45n pvdd 45.5n 0)

Do you see the glitching at the output? Explain what happens. Change the sizes of 2 transistors and fix the glitch-
The glitching is caused due to a race condition that is inherent in the given True Single Phase Flip-Flop. To see this race condition consider what happens if D is low. When CLK is low A is precharged high through M2, then when CLK transitions from low to high device M6 turns on which causes A to begin discharging through M4 & M6. In addition, both M9 and M10 will also be on while A is discharging, causing B to initially discharge which in turn causes the output to glitch. Once A has been discharged B will be pulled high through M7. In order to correct this problem we need to resize the pull-down path through M4 and M6 to cause A to discharge much more quickly. With the current sizing the pull-down path through M9 and M10 is much stronger and therefore allows the glitching.

Our approach, used for the graphs provided in the solutions, is to reduce the strength of the M9 and M10 pull-down path by decreasing their widths. Another is to speed up the M4 and M6 pull-down path increasing their widths.

<table>
<thead>
<tr>
<th>Technique</th>
<th>Old Sizes</th>
<th>New Sizes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow down pull-down path through M9 &amp; M10</td>
<td>M9=8/2, M10=8/2</td>
<td>M9=3/2, M10=3/2</td>
</tr>
<tr>
<td>Speed up pull-down path through M4 &amp; M6</td>
<td>M4=4/2, M6=4/2</td>
<td>M4=12/2, M6=12/2</td>
</tr>
</tbody>
</table>

Glitching on B & Q with OLD Sizing

Glitching on B & Q with NEW Sizing
For the corrected flip-flop, the setup time was measured to be 200 ps. Note that you need to measure the setup time for both values of D, and quote the worst case. It is possible for the setup time for D=1 to be negative because the data can still be sampled after CLK goes to 0.

\[ T_{su} = 200 \text{ ps} \]

Problem 4: Sequential Circuit

Consider the following sequential circuit. Assume that there is no delay between \( D \) and \( \overline{D} \) (i.e., the inverter delay to obtain \( \overline{D} \) from \( D \) is 0). Assume that the output is statically held using circuits not shown here (i.e., ignore leakage effects for this problem). Assume that the rise/fall times on all signals are zero.
a) Complete the following timing diagram for X and Q.

Assume that the inverter delay is much smaller than the clock period and that appropriate set-up/hold times are met. Assume that each gate (I₁, I₂, I₃, NOR, M₁-M₄ and M₇-M₁₀) takes 1 time unit for a low to high or high to low transition. Also assume that it takes 1 time unit to charge node X through M₅ or M₆. Both the propagation and contamination (i.e., minimum) delay are equal to 1.

b) What is the set-up time for this circuit if glitches on the output Q are acceptable? Explain.

**Solution**

The circuit is a pulse-register. For the circuit to function properly, the value of D to be sampled must be able to propagate to X, then to Q, during the window CLK and CLKDB are both high.

To sample D correctly, X must charge/discharge 1 unit before CLKDB=0 and D must be ready 2 time units before CLKDB=0. Therefore, \( t_{su} = -1 \).

Problem 5: DEC StrongARM Low Power Edge-Triggered Flip-Flop

The flip-flop shown in the above figure is used in the StrongARM microprocessor developed by Digital Equipment Corporation for the Portable Electronic Device (PED) market. Note that it is fully differential. The following questions will help you understand the operation of this flip-flop. No calculations are necessary for this problem.

a) When clock is low is the flop holding or is it transparent? Why? (2 sentences)

Solution

The flip-flop is in the hold state while the clock is low as the two PMOS pull-ups are turned on and this pulls the inputs to the cross-coupled NAND gates high, which in turn causes them to hold their previous state.

b) What is the purpose of the shorting transistor connecting nodes L3, L4? (2 sentences)

Solution

The shorting transistor is used to provide a DC leakage path from either node L3 or L4 to ground. This is necessary when the inputs change their value after the positive edge of CLK has occurred, resulting in either L3 or L4 being left in a high-impedance state with a logical low voltage level stored on the node. Without the leakage path this node would be susceptible to charging by leakage currents through the corresponding PMOS device onto either L1 or L2, as a result the latch could actually change state prior to the next rising edge of CLK! This is best demonstrated by example shown in the following figure.
c) What is the main advantage of this flip-flop from a low power perspective? (1 sentence)

Solution

The main advantage is that the clock is only connected to 3 MOS devices (2 PMOS + 1 NMOS).

d) What determines the setup time for this flip-flop? Draw a timing diagram showing the timing relationship between the data and the clock. (1 sentence)

Solution

This register has no setup time. The master only samples at the clock edge. The hold-time is determined by the amount of time it takes the input sense-amplifier structure to discharge either L3 or L4 (L3 if IN = 1, L4 if IN = 0).

e) From a system perspective, where should this flip-flop be used (i.e., in datapaths for pipelining, as receivers at the end of long buses, as state bits for FSMs, etc.)? Why? (1 sentence)

Solution

The sensitivity of the input sense-amp, and its very short setup times, makes this flip-flop best suited for use as a receiver at the end of a long bus.

Problem 6: Submicron Interconnect Effects.

Consider the following interconnect circuit. $C_L$ is the lumped capacitance of each line to ground and $C_I$ is the inter-wire capacitance. The driver (inverter) is modeled using resistors and an ideal switch. The Switch is ideal and is connected either to the top resistor or the bottom resistor. $R_I$ is the effective resistance of the interconnect. For this problem, let $\lambda = \frac{C_I}{C_L}$. 
a) Assume that the initial voltage on line \(i\) (where \(i = 0\) or \(1\)) is \(V_i^{OLD}\) and the final value after all the transients have settled is \(V_i^{NEW}\). Derive an expression for the energy drawn from \(V_{DD}\) through driver 0 for an arbitrary transition of the two bit bus.

**Solution**

\[
E_{drawn}^0 = \int (V_0^{NEW} \cdot i) dt
\]

\[
= V_0^{NEW} \left( \int C_L \frac{dV}{dt} dt + \int C_I \frac{d(V_0 - V_1)}{dt} dt \right)
\]

\[
= V_0^{NEW} \left( C_L (V_0^{NEW} - V_0^{OLD}) + C_I (V_0^{NEW} - V_0^{OLD}) - C_I (V_1^{NEW} - V_1^{OLD}) \right)
\]

**Note 1:** if \(V_0^{NEW} = 0\), No energy is drawn from the driver 0.

**Note 2:** It is possible for \(E_{drawn}^0 < 0\) if current goes into the power supply. Note total energy drawn must be positive, so \(E_I^{drawn} > 0\), if \(E_{drawn}^0 < 0\). See this in part (c).

b) Assume that \(\lambda = 0\) for this part. The total energy (i.e., including both drivers) drawn from the power supply for a sequence can be written as \(\eta \cdot C_L \cdot V_{DD}^2\). Estimate the value of \(\eta\) for the following two sequences.

**Sequence A:** 00 \(\rightarrow\) 01 \(\rightarrow\) 11 \(\rightarrow\) 10

**Solution**

00 \(\rightarrow\) 01, \(E_I = 0, E_0 = C_L V_{DD}^2\),

01 \(\rightarrow\) 11, \(E_I = C_L V_{DD}^2, E_0 = 0\),

11 \(\rightarrow\) 10, \(E_I = 0, E_0 = 0\)

\(E_{total} = 2C_L V_{DD}^2, \eta = 2\)
**Sequence B:** 00 → 11 → 00

**Solution**

00 → 11, \( E_I = E_0 = C_L V_{DD}^2 \),

11 → 00, \( E_I = E_0 = 0 \),

11 → 10, \( E_I = E_0 = C_I V_{DD}^2 \)

\[ E_{\text{total}} = 4C_L V_{DD}^2, \eta = 4 \]

c) Assume that \( \lambda = 3 \) for this part. The total energy (i.e., including both drivers) drawn from the power supply for a sequence can be written as \( \eta \cdot C_L \cdot V_{DD}^2 \). Estimate the value of \( \eta \) for the following two sequences.

**Sequence A:** 00 → 11 → 10

**Solution**

00 → 01, \( E_I = 0, E_0 = C_L V_{DD}^2 + C_I V_{DD}^2 \),

01 → 11, \( E_I = C_L V_{DD}^2 + C_I V_{DD}^2, E_0 = -C_I V_{DD}^2 \),

11 → 10, \( E_I = C_I V_{DD}^2, E_0 = 0 \)

\[ E_{\text{total}} = 2(C_L + C_I) V_{DD}^2, \eta = 8 \]

**Sequence B:** 00 → 01 → 00

**Solution**

Sequence B is exactly the same as in (b) because \( C_I \) never gets charged or discharged, \( \eta = 4 \)

Explain any differences from part (b)

Sequence A in (c) is more because \( C_I \) is being charged or discharged each cycle.

**d)** For the transition of the bus from 01 to 10, compute the total energy dissipated in the resistors.

**Solution**

Using (a)

\[ E = V_{DD}^2 (C_L V_{DD}^2 + C_I V_{DD}^2) - C_I (0 - V_{DD}) = (C_L + 2C_I) V_{DD}^2 \]

\( E_0 = 0 \)

Energy stored in circuit is the same before and after.

So, \( E_{\text{dissipated}} = E_{\text{drawn}} - \Delta E_{\text{stored}} = 2(C_L + C_I) V_{DD}^2 \).
Problem 7: Data-Dependent Logic Swing Internal Bus Architecture (DDL Bus)\(^1\)

Consider the DDL bus architecture for an N bit bus. (Refer to the figures in the lecture notes.)

a) Assuming M bits switched to 0, by what factor do we save power compared to the conventional full swing bus? (remember that there are always 2 bits switching to 0 to provide the “0” and “1” references)

Solution

The savings can be computed using the following analysis:

\[ E_{\text{conventional}} = M \cdot C \cdot (V_{DD})^2 \]

\[ E_{\text{DDL}} = (M + 2) \cdot C \cdot V_{DD} \cdot V_{\text{swing}} = C \cdot \frac{M + 2}{M + 3} \cdot (V_{DD})^2 \quad V_{\text{swing}} = \frac{1}{M + 3} \cdot V_{DD} \]

\[ \therefore \frac{E_{\text{conventional}}}{E_{\text{DDL}}} = \frac{M + 3}{M + 2} \cdot \frac{M}{M} \]

shows the receiver for the DDL bus architecture. (Dual Reference Sense Amplifying Receiver)

b) What is the range of “0” ref? Why are there two “0” refs?

Solution

The range of “0” ref is defined by the two boundary cases when no bits switch to 0, and when all bits (i.e., N) switch to 0. The resulting range is thus:

\[ \frac{2}{3} V_{DD} < V_{\text{ref}} < \frac{N + 2}{N + 3} \cdot V_{DD} \]

The reason for having two “0” refs is to generate the “1” ref. The worst case “1” that can occur in the DDL bus is when the adjacent two bus wires switch to 0. This results a voltage drop on the precharged “1” because of the coupling capacitance between the wires. The circuit is providing this worst case by always making two bits switching 0 (“0” ref and “0” ref+) and placing a dummy wire (“1”) between them (consult the figure in the lecture notes for further reference).

c) What is the reason for having M2 and M3? Wouldn’t it be enough just to have M1 and M4 charge up the nodes A and B to turn the inverter off during precharge?

Solution

If we only have M1 and M4, the cross coupled inverter will be turned off by M1 and M4 but the internal nodes out, out won’t be at the same voltage level. During the evaluation phase, this voltage difference immediately forces the cross coupled inverter to go to a steady state independent of the current pulled down from nodes A and B, hence the input data. Therefore, precharging the internal nodes out, out is necessary and M2, M3 are needed.

The following figure shows the receiver for the DDL bus architecture. (Dual Reference Sense Amplifying Receiver)

Dual reference sense amplifying receiver.
Project Report

• Template is posted on the course web page (two column and **TWO pages MAX**)

• One page of Text (2 column):
  – Clearly introduce the problem and why it is important
  – Describe and cite previous work (2-3 references)
  – Describe your basic contribution and ideas (make sure you indicate what parts worked and what parts did not work)
  – Describe the three most innovative ideas pursued in your project (even if it does not work!)
  – Any suggestion for future work

• One page of Figures (2 column - 8 figures max)
  – Overview (e.g., block diagram of system)
  – 3 or 4 detailed (circuit schematics or architecture issues)
  – 3 or 4 simulations
  – Include a path for your simulations (make sure we have the appropriate permissions on athena)

• Turn in **four** copies of the 2-page report and the technical summary sheet
Project Presentation

- Schedule will be sent via email this week:
  - 12/9 (in class and from 5:30-7PM)
  - Mail Alex your final project title and team member names.

- Time per group: 10 minutes for a two student team and 15 minutes for a 3 person team. This includes Q & A.

- Content
  - Clearly introduce the problem and what has previously been done
  - Describe your basic contribution and ideas
  - Describe the three most innovative ideas pursued in your project
  - What is the impact of your project (e.g., Factor of 10 reduction in Power without loss in performance, etc.)
  - Pick one or two interesting simulations to show

- Provide us with one hardcopy of the viewgraphs presented.

- Everyone is expected to make a presentation
6.374 Final Project - Technical Summary Sheet

You may complete this form by hand. Please use ONLY the space provided.

Project Title: ______________________________________________________

Authors: ______________________________________________________

List the three most innovative ideas of your project.

1. ________________________________________________________________
2. ________________________________________________________________
3. ________________________________________________________________

List the contributions of each partner.

1. ________________________________________________________________
2. ________________________________________________________________
3. ________________________________________________________________

Provide a path to your files on the class server and provide instructions on how to run the simulations if necessary.

__________________________________________________________________
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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Sciences

Analysis and Design of Digital Integrated Circuits (6.374) - Fall 2003 Quiz #1
Prof. Anantha Chandrakasan

Student Name: ____________________________

Problem 1 (30 Points): _____________________
Problem 2 (24 Points): _____________________
Problem 3 (18 Points): _____________________
Problem 4 (28 Points): _____________________
Total (100 Points): ______________________

Use the following device parameters unless otherwise specified:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{T0}$</td>
<td>0.4 V</td>
<td>0.4 V</td>
</tr>
<tr>
<td>$K' = \mu C_{ox}$</td>
<td>75 µA/V$^2$</td>
<td>25 µA/V$^2$</td>
</tr>
<tr>
<td>$V_{DSAT}$</td>
<td>0.5 V</td>
<td>-0.75 V</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>0.3V$^{1/2}$</td>
<td>-0.3V$^{1/2}$</td>
</tr>
<tr>
<td>$</td>
<td>2\varphi</td>
<td>$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Also assume that all NMOS device bulks are connected to 0V and PMOS well terminals are connected to $V_{DD}$.

STATE ANY ASSUMPTIONS YOU MAKE IN SOLVING PROBLEMS and SHOW YOUR WORK. Points might be taken off if you don’t explain how you arrived at your answer.

There are 13 pages in total
**Problem 1: Driver Circuit:** Consider the following circuit driving a capacitive load of 1pF.

![Circuit Diagram]

- **$V_{DD} = 2.5V$**
- **$C_L = 1pF$**
- **$V_{low} = 1V$**

(a) Assuming that $In$ swings from rail-to-rail (0 to 2.5V), what is the swing on the node $Out$? **(2 points)**

(b) At the switching threshold $V_M = 1.75V$, what is the mode of operation for $M_1$ and $M_2$. Show your work **(4 points)**
(c) Assuming \( \frac{W}{L} = 25\mu m/0.25\mu m \), determine \( \frac{W}{L} \) such that \( V_M = 1.75V \). (6 points)
(d) Assuming \((W/L)_{2} = 25\mu m/0.25\mu m\), determine the low-to-high propagation delay using the method of equivalent RC. Assume that the input switches from 2.5V to 0V with a zero fall time (8 points)
(e) Assuming that the input switches at a clock frequency of 100MHz with a swing of 0 to $V_{DD}$ (with zero rise and fall times) what is the average power dissipation of this circuit? Show your work (10 points).
Problem 2: Pass Transistor Logic

(a) Consider the following circuit implemented using NMOS and PMOS pass transistors. Assume that the inputs and their complements ($A, \bar{A}, B, \bar{B}$) swing rail-to-rail (0 to $V_{DD}$). What is the function implemented by the two circuits. (6 points)

(b) Assuming that the primary inputs ($A, B, C, D$) and their complements have rail-to-rail swing (0 to $V_{DD}$), what is the voltage swing on outputs $Y$ and $Z$? (4 points)
(c) Using the same style of logic in part 2(a) (i.e., using NMOS, PMOS pass transistors connected to signal or $V_{DD}$/GND), create the minimal transistor implementation of the OR/NOR function. Your implementation should have the same swing as the circuits in 2(a) (6 points)
Consider the following cross-coupled complementary pass-gate logic

(d) What is the logic function $Y$ implemented by the above gate? What is the voltage swing on nodes $Y$ and $\overline{Y}$? (4 points)

(e) Assume that $A$, $\overline{A}$, $B$, $\overline{B}$ are from ideal voltage sources and have a rail-to-rail swing (0 to $V_{DD}$). Also assume (just for this part) that there is no body effect ($\gamma = 0$) and ignore sub-threshold conduction. Is this a ratioed circuit? Explain. (4 points).
**Problem 3: Dynamic Logic**

(a) Complete the circuit schematic of the DCVSL gate below (6 points)

(b) What is the function of $M_{p1}$ and $M_{p2}$? Is this a ratioed circuit? (4 points)
(c) Consider the following function $Y = A + B + C$ implemented using a cascade of two 2-input DOMINO OR gates. Assume that $p(A=1) = 0.1$, $p(B=1) = 0.2$, $p(C=1) = 0.5$. Determine the order of inputs to minimize power dissipation (show numerical analysis). Explain. Fill in the empty boxes with the appropriate inputs. (8 points)
**Problem 4: Multiple Threshold CMOS Circuits:** This problem explores issues related to leakage in MTCMOS circuits. **Just for this problem,** assume that the low threshold NMOS and PMOS devices have the following device properties (ignore DIBL). All low-$V_T$ and high-$V_T$ devices are $1\mu m/0.25\mu m$.

<table>
<thead>
<tr>
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<tr>
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<td>-0.3V</td>
</tr>
<tr>
<td>$V_{Thigh}$</td>
<td>0.5V</td>
<td>-0.5V</td>
</tr>
<tr>
<td>$</td>
<td>I_o</td>
<td>$ for a $1\mu m/0.25\mu m$ Device ($V_{GS}=V_T$)</td>
</tr>
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<td>$</td>
<td>S</td>
<td>$ (Sub-threshold slope)</td>
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Consider the circuit shown below (low threshold devices are shaded).

(a) During active mode (SLEEP = 0), provide the logic function for Out (4 points)
(b) Assuming SLEEP = 0 (Active mode), compute the total leakage when A=0, B=0? A numerical result is expected. Draw all the contributing leakage paths on the figure below (10 points)
(c) Assuming SLEEP = 1 (Sleep mode) and A=0, B=1. In the Sleep mode, ideally, the leakage should be small and be set by high-threshold devices. Unfortunately, this is not always the case for distributed sleep devices as shown below. Identify (but do not compute) any leakage path(s) from $V_{DD}$ to ground which are determined by low-threshold devices (i.e., not cut-off by high-threshold devices). (8 points)

(d) For the same assumption of part (c), what do you expect the leakage through device M9 to be:
   (1) 10pA
   (2) 1nA
   (3) >> 1nA
Briefly explain why (6 points)
Analysis and Design of Digital Integrated Circuits (6.374) - Fall 2003 Quiz #2
Prof. Anantha Chandrakasan

Student Name: ____________________________

Problem 1 (30 Points): ____________________
Problem 2 (24 Points): ____________________
Problem 3 (22 Points): ____________________
Problem 4 (24 Points): ____________________

Total (100 Points): ______________________

For the entire quiz, ignore body effect ($\gamma=0$) and leakage effects. Also assume that all NMOS device bulks are connected to 0V and PMOS well terminals are connected to $V_{DD}$.

STATE ANY ASSUMPTIONS YOU MAKE IN SOLVING PROBLEMS and SHOW YOUR WORK

There are 13 pages in total
**Problem 1: Carry Skip Adder:** In this problem, we will explore the addition of two numbers based on the Carry Skip (or Carry Bypass) technique.

a) Consider the following 16-bit Carry Skip Adder. Assume that the Sum Logic (SL) block for stage $i$ has as inputs $P_i$, $G_i$, and $C_{in,i}$. Assume the following delays:

- Delay to produce the $P_i$, $G_i$ signals from the $A_i$, $B_i$ inputs is 1 (i.e., the delay of the PG_L block)
- Delay to compute $C_{out,i}$ from $P_i$, $G_i$ and $C_{in,i}$ inputs is 1 (i.e., the delay of the Carry Logic (CL) block)
- Delay to compute $S_i$ from $C_{in,i}$, $P_i$, $G_i$ being valid is 2 (i.e., the delay of the Sum Logic (SL) block)
- Delay for the 2:1 multiplexor is 2
- Delay to compute the group propagate, $GP_i$, is 1 (assume for the entire problem that this delay is independent of the fan-in)

Highlight the critical path for this 16-bit adder directly on Figure 1 (4 points)

![Figure 1: A 16 bit Carry Skip Adder with a block size $M = 4$.](image)

(b) What is the delay for a 32-bit adder assuming equal block sizes of 4 and making the same assumptions of delay as 1 (a)? (4 points)
(c) Consider an $N$-bit Carry Skip adder with equal block sizes of $M$-bits. With the same timing assumptions of 1(a), derive the optimum block length $M$, for an $N$-bit adder. (6 points)

(d) Consider a transmission gate implementation of a 4-bit Carry-Skip section. Derive the signals $S_1$, $S_2$, and $S_3$ as a function of $P_i$ and $G_i$. Will this circuit work if $P_i = A + B$? Explain. (8 points)

Figure 2: A transmission gate implementation of a 4-bit Carry Skip section.
(e) Consider the following 32-bit adder variation where the block sizes of each stage are not equal. Highlight the critical path directly on Figure 3. What is the delay of the critical path? (8 points)

Figure 3: A 32-bit Carry Skip Adder with a variable block size.
Problem 2: Sequential Element: Consider the following circuit. Assume that each inverter takes 1 time unit for a low-to-high or high-to-low transition. Assume that it takes 1 time unit for a pull-up path or pull-down path to pull-up or pull-down, respectively. Ignore any leakage effects. Assume $V_{DD} \gg V_T$. Also assume that there is no skew between $CLK$ and $\overline{CLK}$ and assume that the rise/fall times on all signals are zero.

(a) Complete the timing diagram below. What type of sequential element is the above circuit? Be specific. (8 points)
(b) What is the setup time, $t_{su}$, hold time, $t_{hold}$ and propagation delay, $t_p$ of this sequential building block relative to the appropriate edge(s)? Explain. (6 points)
(c) Consider the following simple sequential system built using the sequential element in Figure 4. Assuming that there is no skew in distributing the clock, what is the minimum possible clock period for which this sequential system will function? Assume that the primary input $In$ is setup before the appropriate clock edge(s). (6 points)

(d) What is the maximum positive skew on the clock to SE2 such that the circuit still functions? (4 points)
**Problem 3: Sequential Circuit:** Consider the following circuit. Assume that each inverter takes 1 time unit for a low-to-high or high-to-low transition. Also assume that it takes 1 time unit for a pull-up path or pull-down path to pull-up or pull-down, respectively. Assume that ratioed circuits are properly sized (i.e., assume that the devices in the cross-coupled inverters are weak and can be overpowered). Assume that the rise/fall times on all signals are zero.

(a) Complete the following timing diagram for QSD, QSD#, END. (8 points)

![Sequential Circuit Diagram](image-url)
(b) Assuming that the circuit of Figure 6 directly drives a dynamic DCVSL gate (i.e., differential N-type dynamic logic clocked by $CLK$), what is the setup time of the circuit in Figure 6 relative to the appropriate clock edge? Explain. (4 points)

(c) What is the hold time, $t_{hold}$ and propagation delay, $t_p$, of the circuit in Figure 6 relative to the appropriate clock edge? (4 points)
(d) Consider the following sequential implementation which includes both differential dynamic logic and static logic. The circuit below has a major problem. Identify the problem and propose a solution (draw a gate level schematic).

(6 points)

![Sequential System Diagram]

**Figure 7:** Sequential System.
Problem 4: Interconnect Issues: For this entire problem assume $C_I/C_L = 5$. ($C_I$ is the interwire capacitance and $C_L$ is the line capacitance to the substrate). An inverter is modeled using resistors and an ideal switch. The switch is connected either to the top resistor or the bottom resistor.
(a) Consider the 2-line bus shown in Figure 8. Compute the total energy drawn from the power supply $V_{DD}$ for the transition of $(I_{n0}, I_{n1})$ from 01 to 10. (6 points)

![Figure 8: 2-bit bus.](image-url)
(b) Consider the following modification in which the inverters are replaced by tri-state inverters. When the enable signal \( En \) is low, the tri-state does not drive the LINE. In addition, a switch with a small resistance \( R \) is added in parallel with \( C_I \) which is closed when the control signal \( S = 1 \). Consider the same transition as 4(a) in which \((In_0, In_1)\) switches from 01 to 10. However, before the transition happens, the switch is shorted and then opened. Assume that the time period when the switch is closed is long enough for all the transients to settle. Compute the total energy drawn from the power supply \( V_{DD} \). \( \text{(8 points)} \)

![Diagram of modified driving scheme for a 2-bit bus.]

**Figure 9:** Modified driving scheme for a 2-bit bus.
(c) Consider the following input sequence, which represents all the possible transitions for 2 input bus.

**Transition Sequence:** $00 \rightarrow 00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 01 \rightarrow 01 \rightarrow 00 \rightarrow 11 \rightarrow 11 \rightarrow 10 \rightarrow 00$

What is the difference in energy drawn from the power supply for the above sequence using the approach in 4(b) vs. 4(a). For the scheme in part 4 (b), assume that you may choose on a transition by transition basis if the switch should be closed before the transition happens. If the switch is closed between transitions, assume that the tri-state driver is off during that period. **(10 points)**